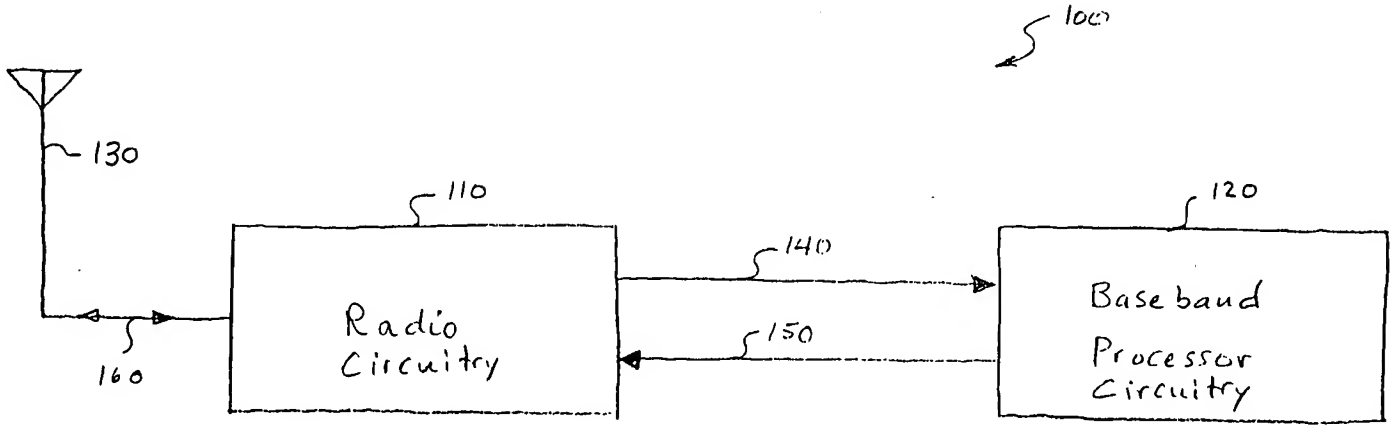
100
130
110
120
140
150
160
Radio Circuitry
Baseband Processor Circuitry

FIG. 1

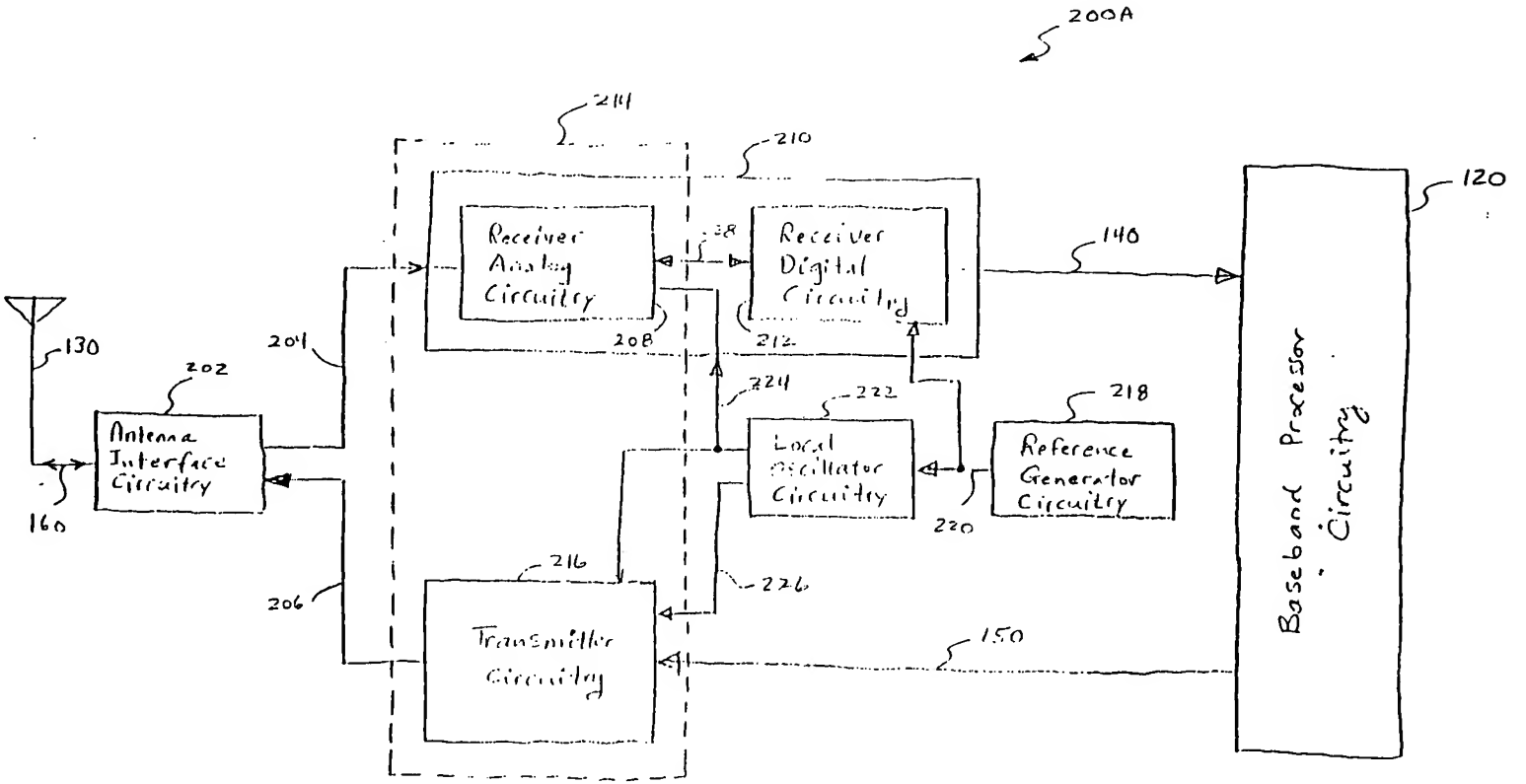
200A
211
210
Receiver Analog Circuitry
208
Receiver Digital Circuitry
212
140
120
Baseband Processor Circuitry
130
160
202
Antenna Interface Circuitry
204
224
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
216
206
226
Transmitter Circuitry
150

FIG. 2A

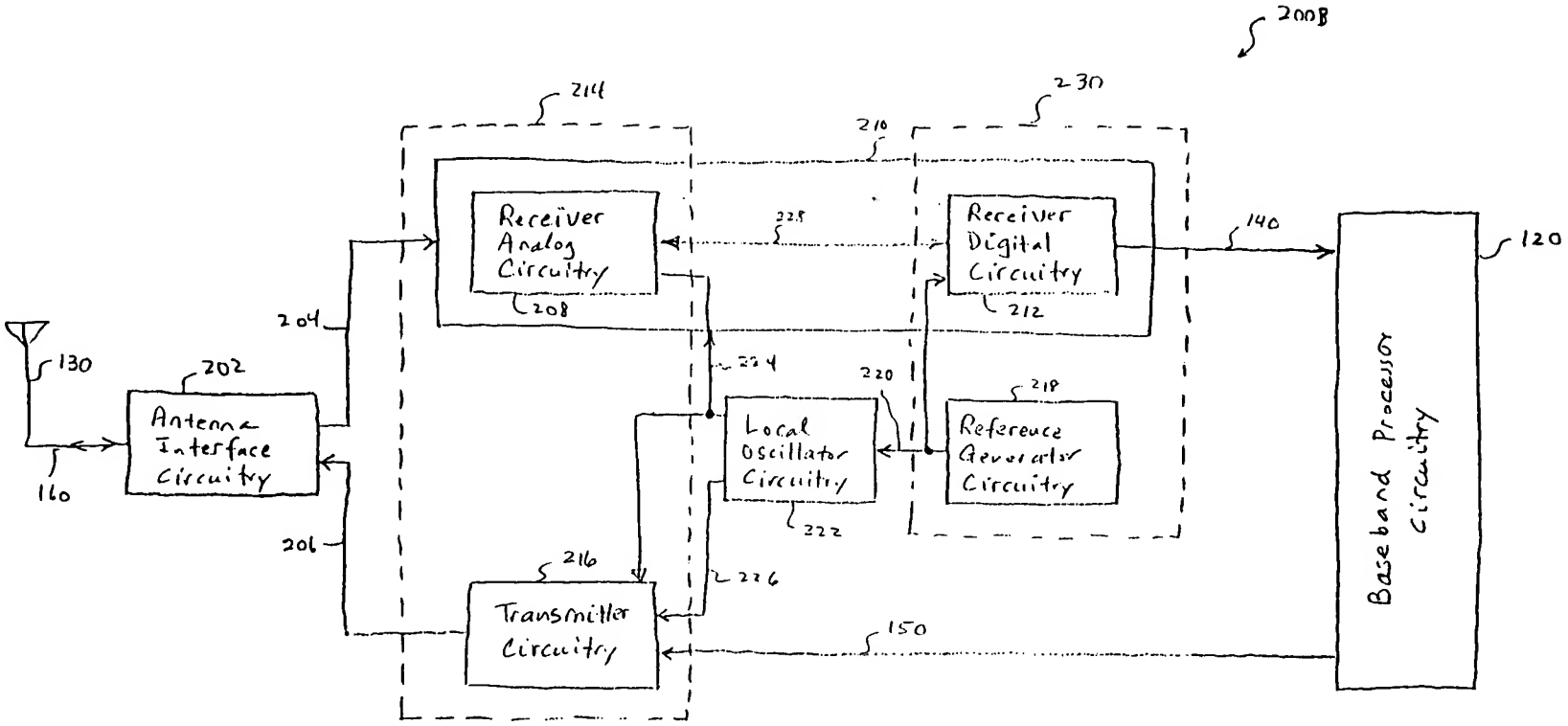
200B
214
230
210
Receiver Analog Circuitry
208
228
Receiver Digital Circuitry
212
140
120
Baseband Processor Circuitry
204
130
202
Antenna Interface Circuitry
160
224
220
218
Local Oscillator Circuitry
222
Reference Generator Circuitry
206
216
226
Transmitter Circuitry
150

FIG. 2B

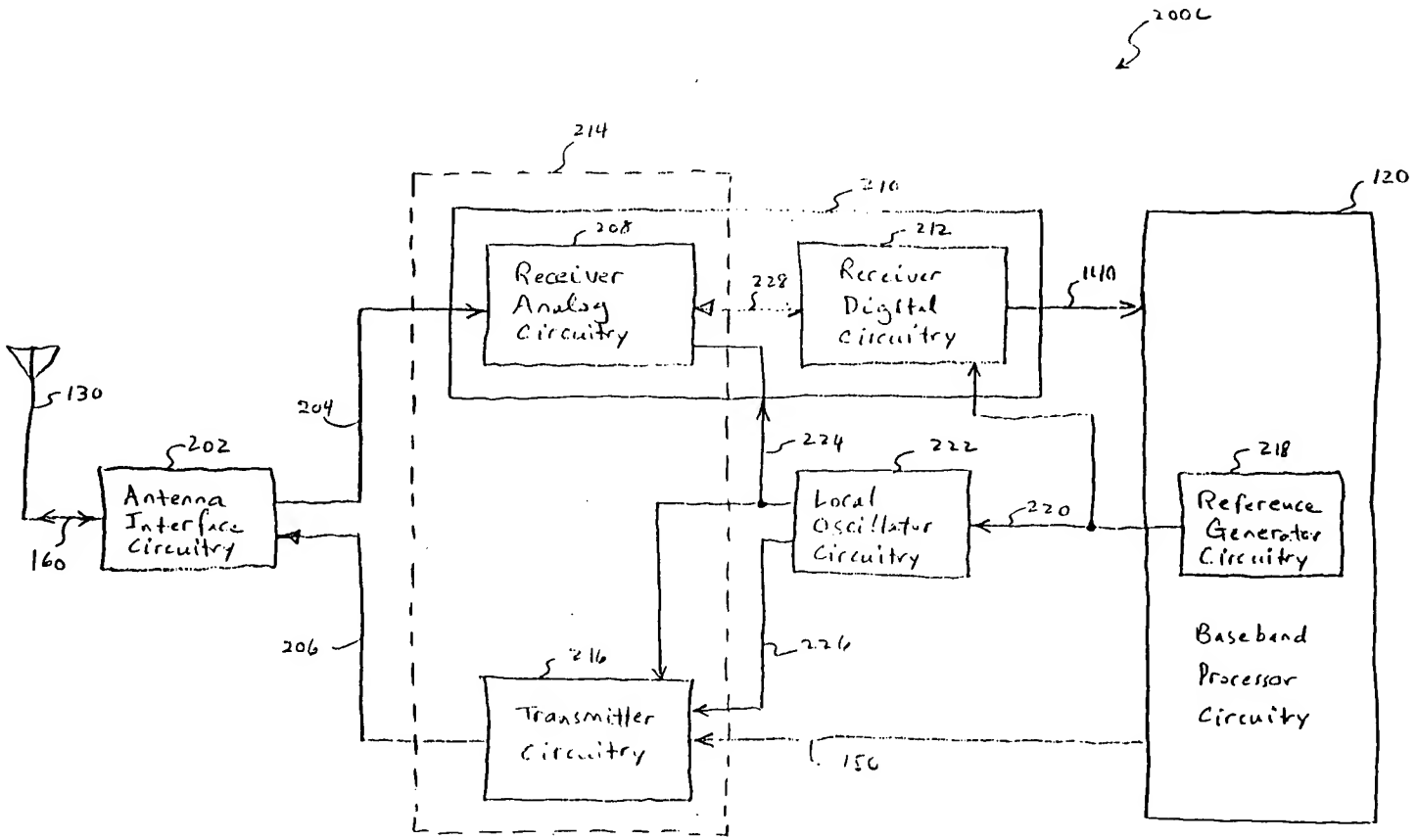
200C
214
210
120
208
212
Receiver Analog Circuitry
228
Receiver Digital Circuitry
114A
130
204
202
224
222
218
Antenna Interface Circuitry
Local Oscillator Circuitry
220
Reference Generator Circuitry
160
206
216
226
Baseband Processor Circuitry
Transmitter Circuitry
156

FIG. 2C

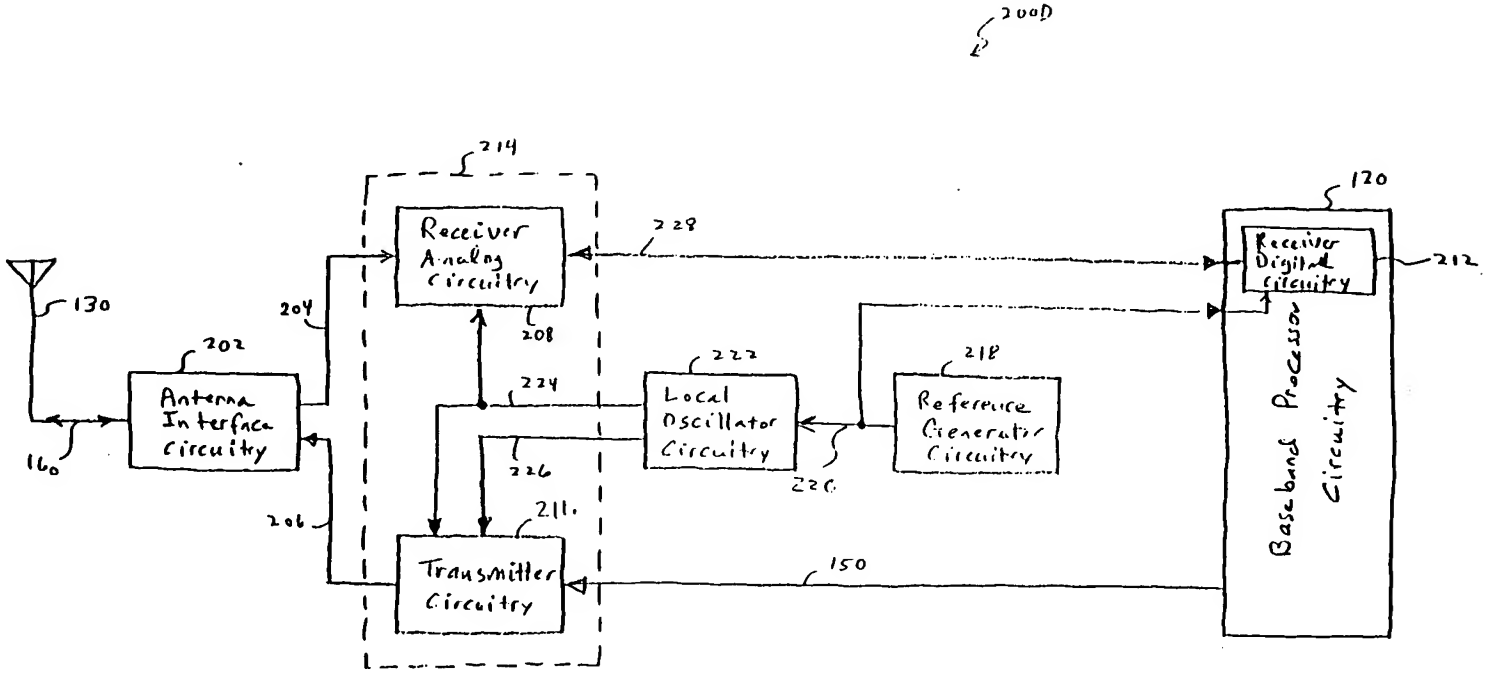
200D
214
Receiver Analog Circuitry
208
228
120
Receiver Digital Circuitry
212
Baseband Processor Circuitry
130
204
202
Antenna Interface Circuitry
160
224
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
226
206
211
Transmitter Circuitry
150

FIG. 2D

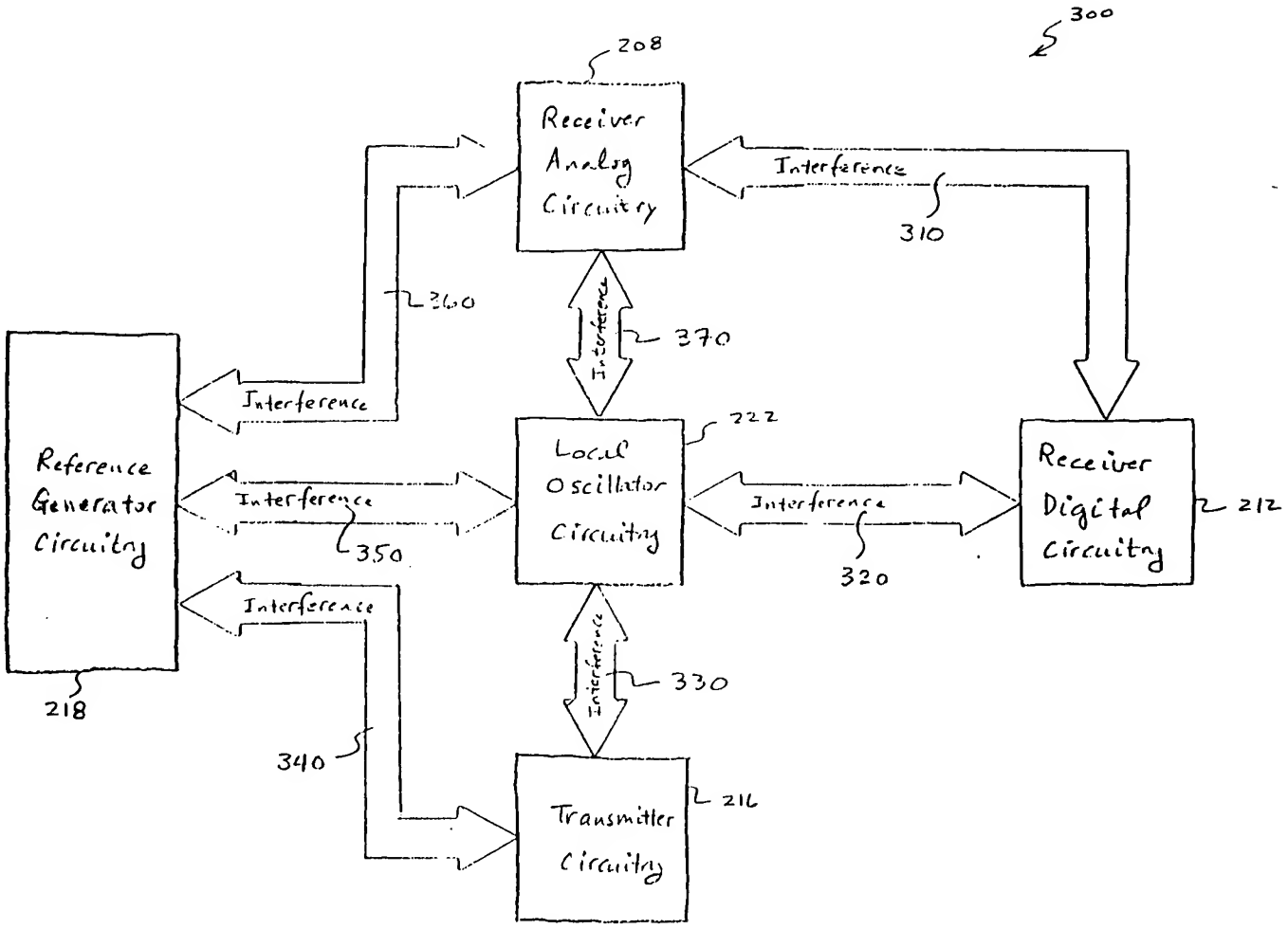
300
208
Receiver Analog Circuitry
Interference
310
360
Interference
370
Interference
Reference Generator Circuitry
Local Oscillator Circuitry
222
Receiver Digital Circuitry
212
Interference
350
Interference
320
Interference
330
218
340
Transmitter Circuitry
216

FIG. 3

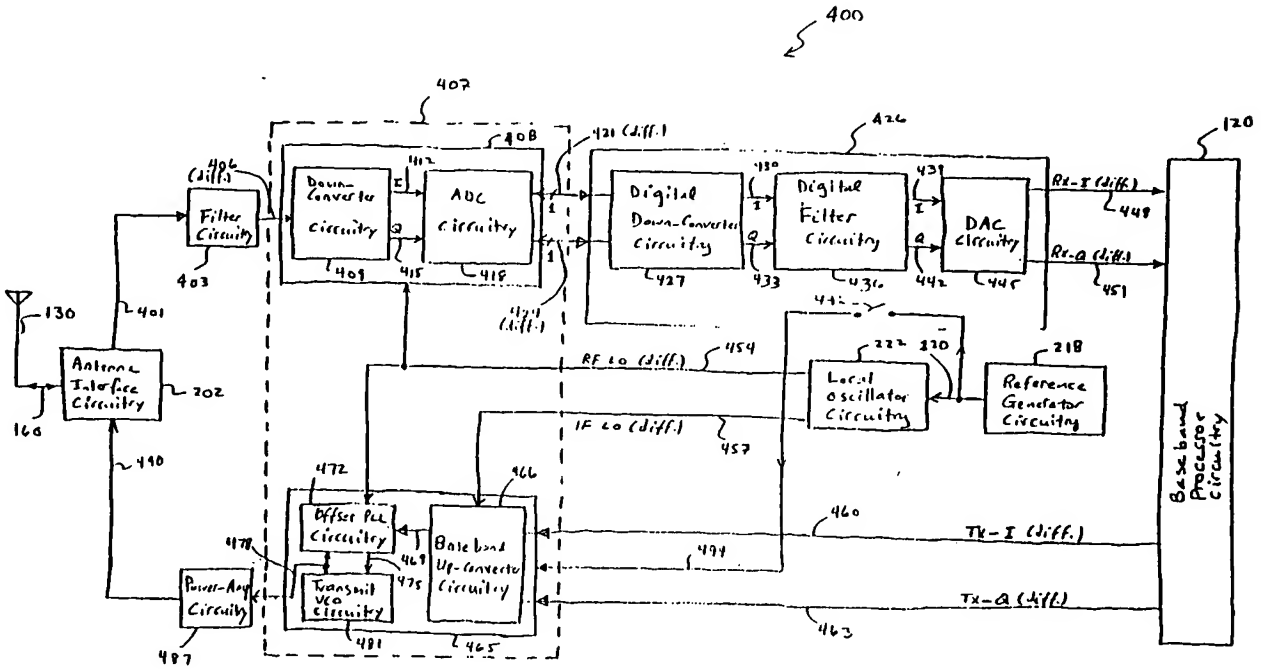
400
407
408
406 (Diff.)
Filter Circuitry
403
Down-Converter Circuitry
409
412
I
Q
415
ADC Circuitry
419
421 (Diff.)
427 (Diff.)
426
Digital Down-Converter Circuitry
427
430
I
Q
433
Digital Filter Circuitry
436
439
I
Q
442
DAC Circuitry
445
Rx-I (Diff.)
449
Rx-Q (Diff.)
451
120
Baseband Processor Circuitry
130
401
Antenna Interface Circuitry
202
160
440
RF LO (Diff.)
454
IF LO (Diff.)
457
Local oscillator Circuitry
222
220
Reference Generator Circuitry
218
472
Offset PLL Circuitry
469
Transmit VCO Circuitry
475
481
466
Baseband Up-Converter Circuitry
465
478
Power-Amp Circuitry
487
460
Tx-I (Diff.)
494
Tx-Q (Diff.)
463

FIG. 4

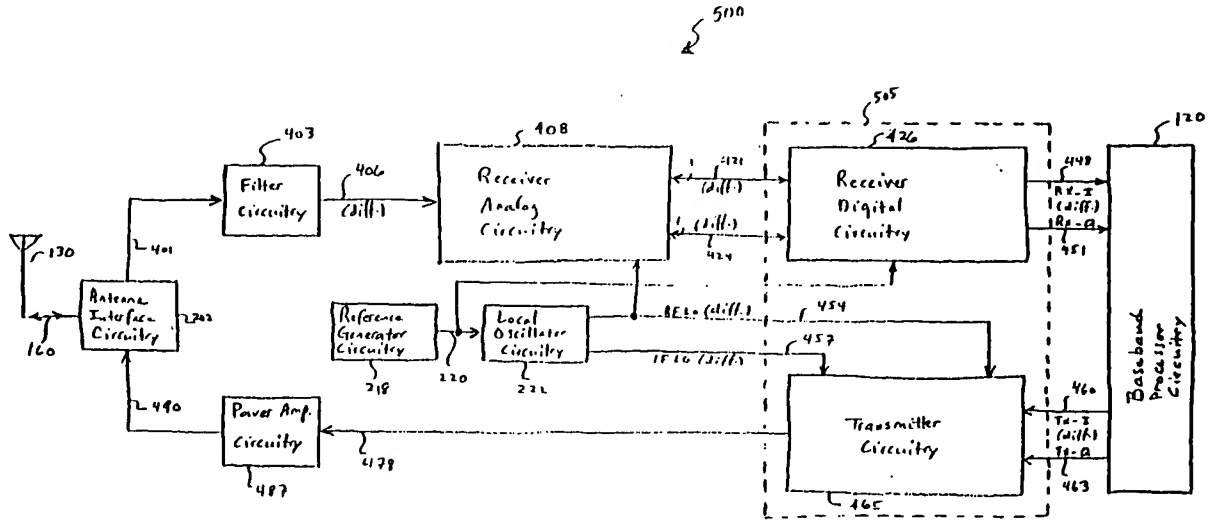
500
505
120
403
408
426
406
Filter Circuitry
Receiver Analog Circuitry
Receiver Digital Circuitry
Baseband Processor Circuitry
130
401
Antenna Interface Circuitry
160
Reference Generator Circuitry
218
220
Local Oscillator Circuitry
222
454
457
Power Amp. Circuitry
478
487
Transmitter Circuitry
460
463
465
451

FIG. 5

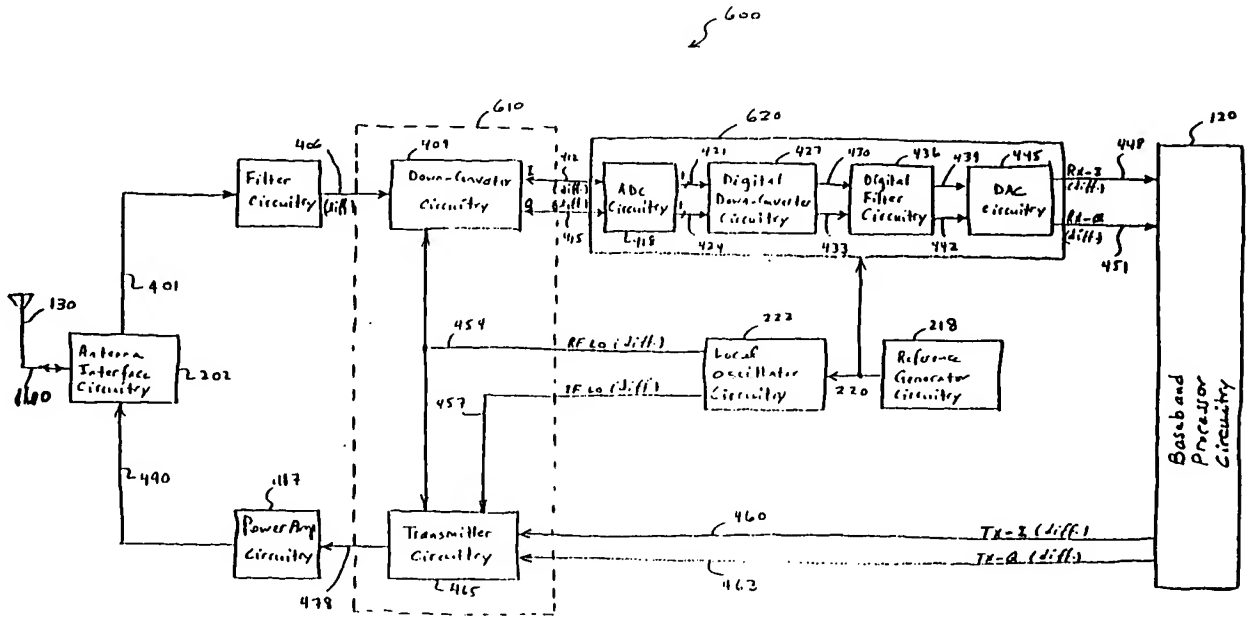
600
610
620
120
406
409
Filter Circuitry
Down-Converter Circuitry
ADC Circuitry
Digital Down-Converter Circuitry
Digital Filter Circuitry
DAC circuitry
Baseband Processor Circuitry
130
401
Antenna Interface Circuitry
202
180
454
RF LO (Diff.)
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
457
IF LO (Diff.)
490
117
Power Amp Circuitry
Transmitter Circuitry
460
Tx-I (Diff.)
Tx-Q (Diff.)
463
478
465
448
451

FIG. 6

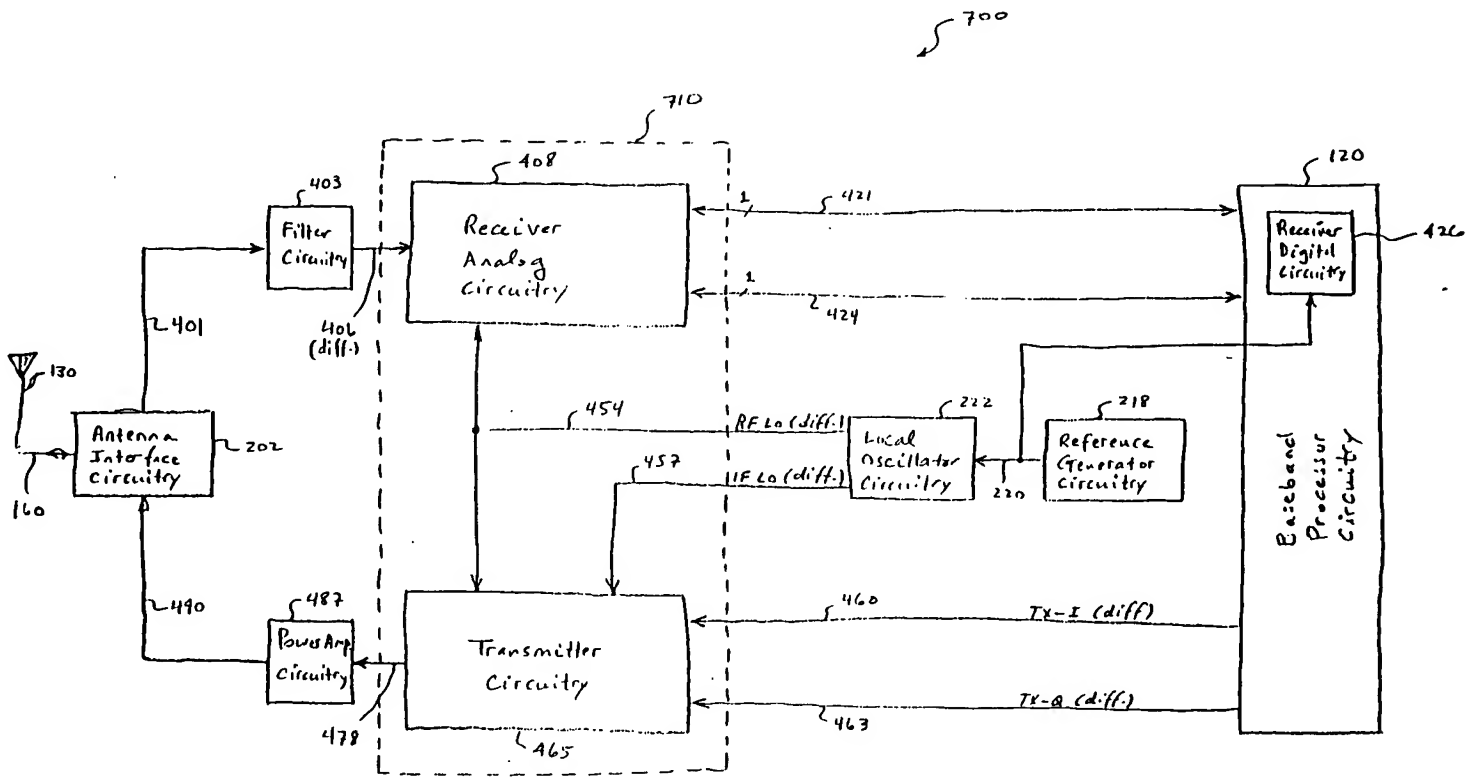
700
710
408
403
Filter Circuitry
Receiver Analog Circuitry
120
Receiver Digital Circuitry
426
421
424
406 (diff.)
401
130
Antenna Interface Circuitry
202
160
454
RF LO (diff.)
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
457
IF LO (diff.)
Baseband Processor Circuitry
490
487
Power Amp Circuitry
Transmitter Circuitry
460
Tx-I (diff)
Tx-Q (diff.)
463
478
465

FIG. 7

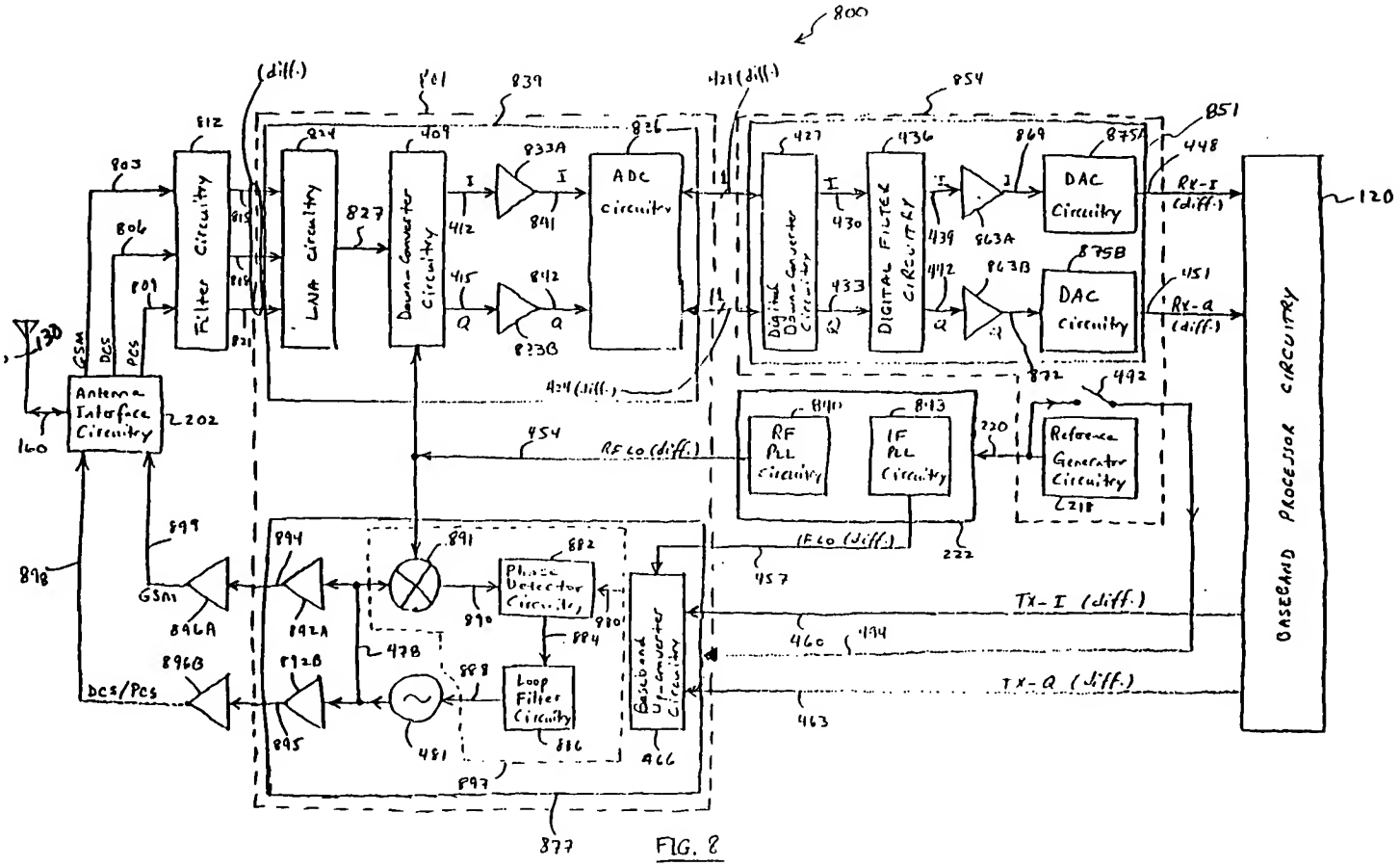
800
(diff.)
839
812
824
409
826
803
806
801
827
I
Q
412
415
841
842
833A
833B
ADC circuitry
Filter Circuitry
LNA circuitry
Down-Converter Circuitry
GSM
DCS
PCS
130
160
Antenna Interface Circuitry
2202
424 (diff.)
421 (diff.)
854
851
427
436
869
875A
875B
448
451
120
Digital Down-Converter Circuitry
DIGITAL FILTER CIRCUITRY
DAC Circuitry
Rx-I (diff.)
Rx-Q (diff.)
430
433
439
863A
863B
872
492
454
RF LO (diff.)
RF PLL circuitry
IF PLL Circuitry
220
Reference Generator Circuitry
2218
222
457
898
899
GSM
896A
894A
891
882
Phase Detector Circuitry
890
880
884
Loop Filter Circuitry
886
888
478B
481
DCS/PCS
896B
895
892B
Baseband Up-converter Circuitry
466
Tx-I (diff.)
460
494
Tx-Q (diff.)
463
BASEBAND PROCESSOR CIRCUITRY
897
877

FIG. 8

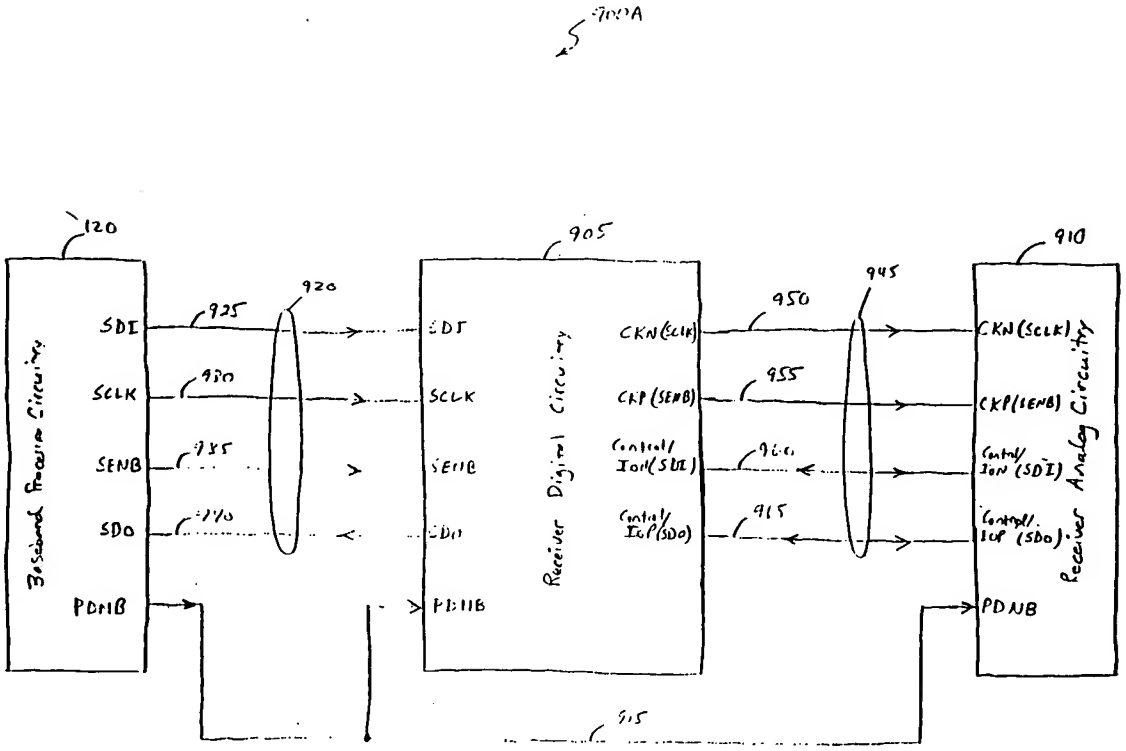
700A
120
905
910
Baseband Processing Circuitry
Receiver Digital Circuitry
Receiver Analog Circuitry
SDI
SCLK
SENB
SDO
PDNB
925
930
935
940
920
945
950
955
960
915
CKN(SCLK)
CKP(SENB)
Control/ IoN(SDI)
Control/ IoP(SDO)
915

FIG. 9A

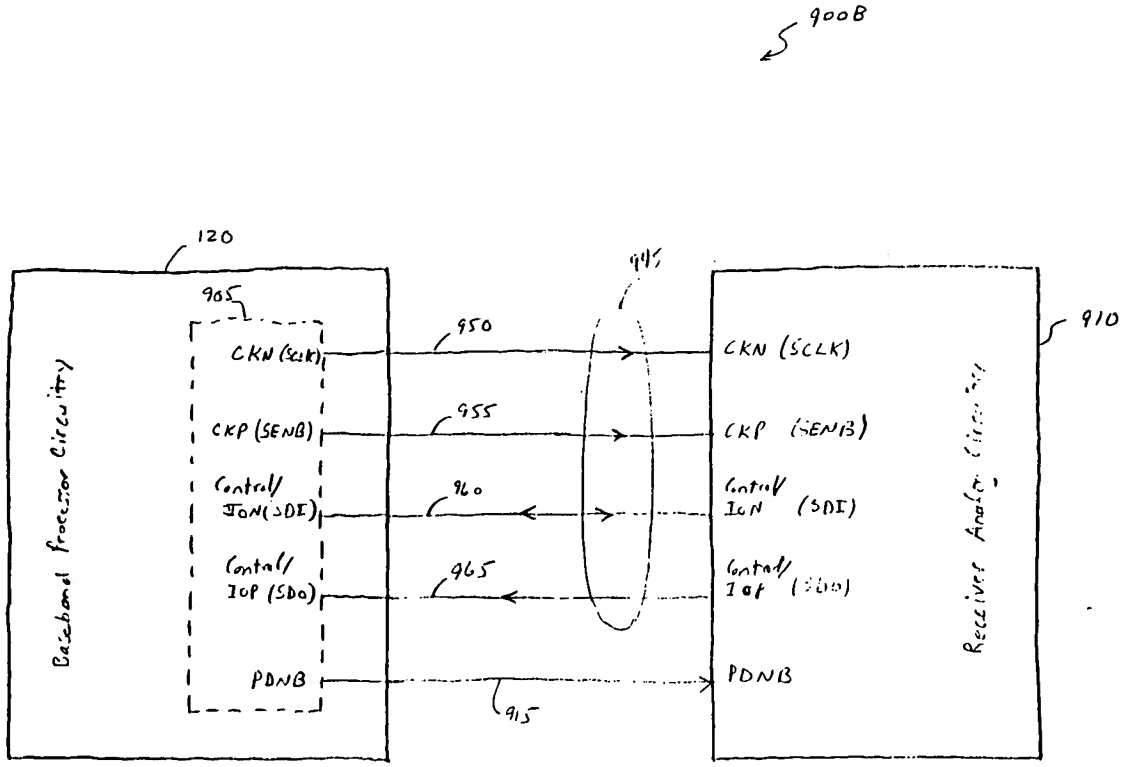
900B
120
905
915
910
950
955
960
965
CKN (SCLK)
CKP (SENB)
Control IoN (SDI)
Control IoP (SDO)
PDNB
CKN (SCLK)
CKP (SENB)
Control IoN (SDI)
Control IoP (SDO)
PDNB
Baseband Processor Circuitry
Receiver Analog Circuitry

FIG. 9B

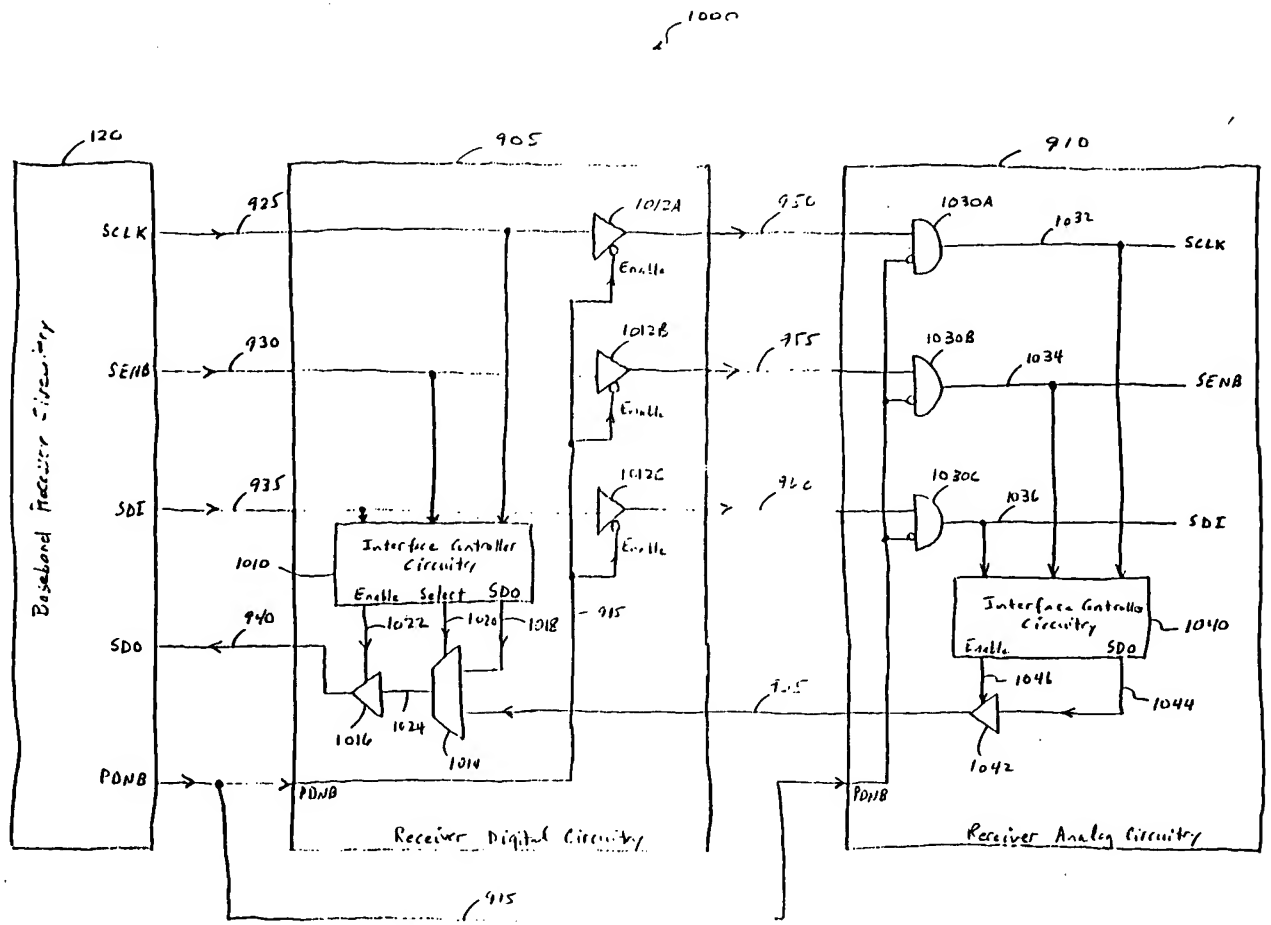
1000
120
905
910
Baseband Receiver Circuitry
SCLK
SENB
SDI
SDO
PDNB
925
930
935
940
915
950
955
960
965
1012A
1012B
1012C
Enable
1010
Interface Controller Circuitry
Enable Select SDO
1022
1020
1018
1016
1024
1014
1030A
1030B
1030C
1032
1034
1036
1040
1046
1044
1042
Receiver Digital Circuitry
Receiver Analog Circuitry

FIG. 10

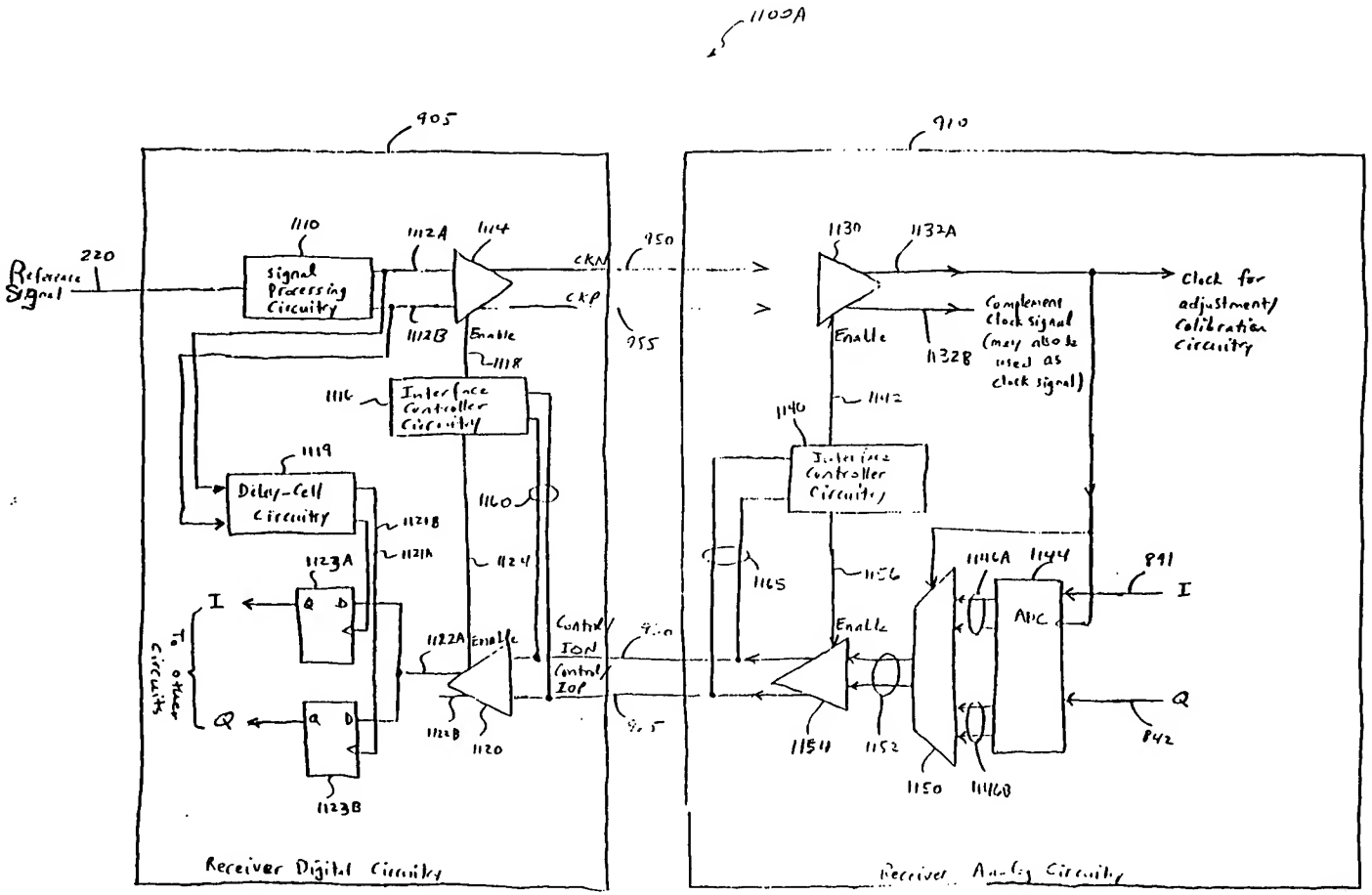
1100A
905
910
Reference Signal
220
1110
Signal Processing Circuitry
1112A
1114
CKN
CKP
950
955
1112B
Enable
1118
1116
Interface Controller Circuitry
1119
Delay-Cell Circuitry
1160
1121B
1121A
1124
1123A
I
Q
D
To other circuits
1122A
Enable
Control ION Control IOP
970
975
1122B
1120
1123B
Receiver Digital Circuitry
1130
1132A
Clock for adjustment/ Calibration circuitry
Enable
1132B
Complement clock signal (may also be used as clock signal)
1140
1142
Interface Controller Circuitry
1165
1156
1116A
1144
841
I
Enable
ADC
Q
842
1154
1152
1150
1116B
Receiver Analog Circuitry

FIG. 11A

20020730 225200T

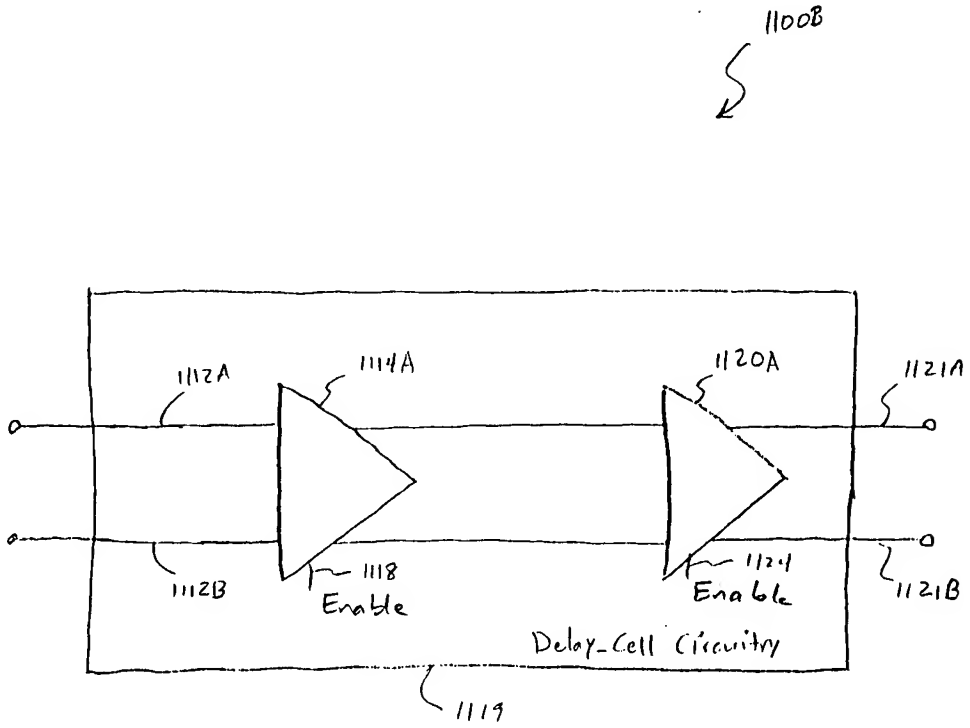

FIG. 11B

20020730 021526OT

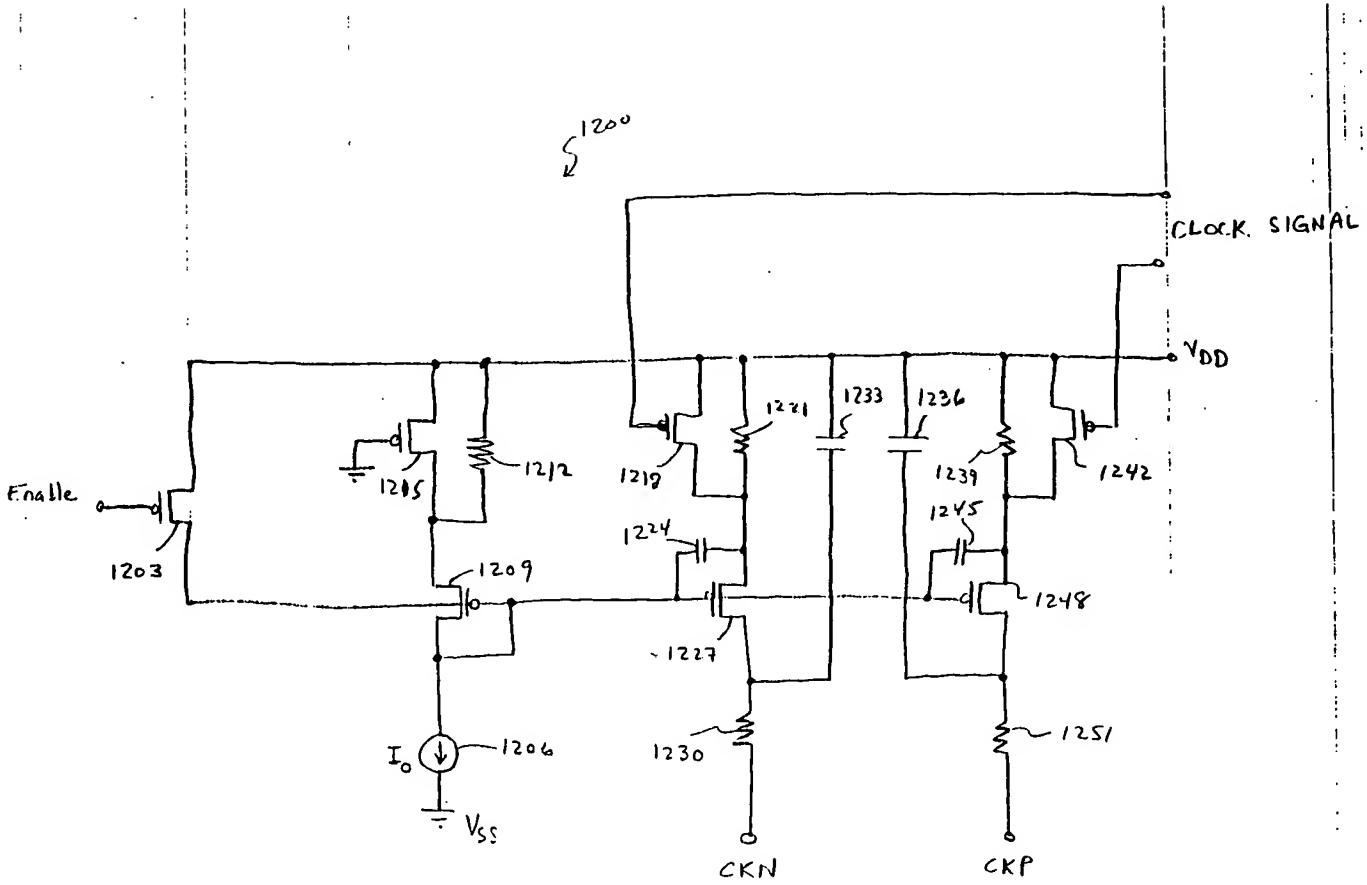

FIG. 12

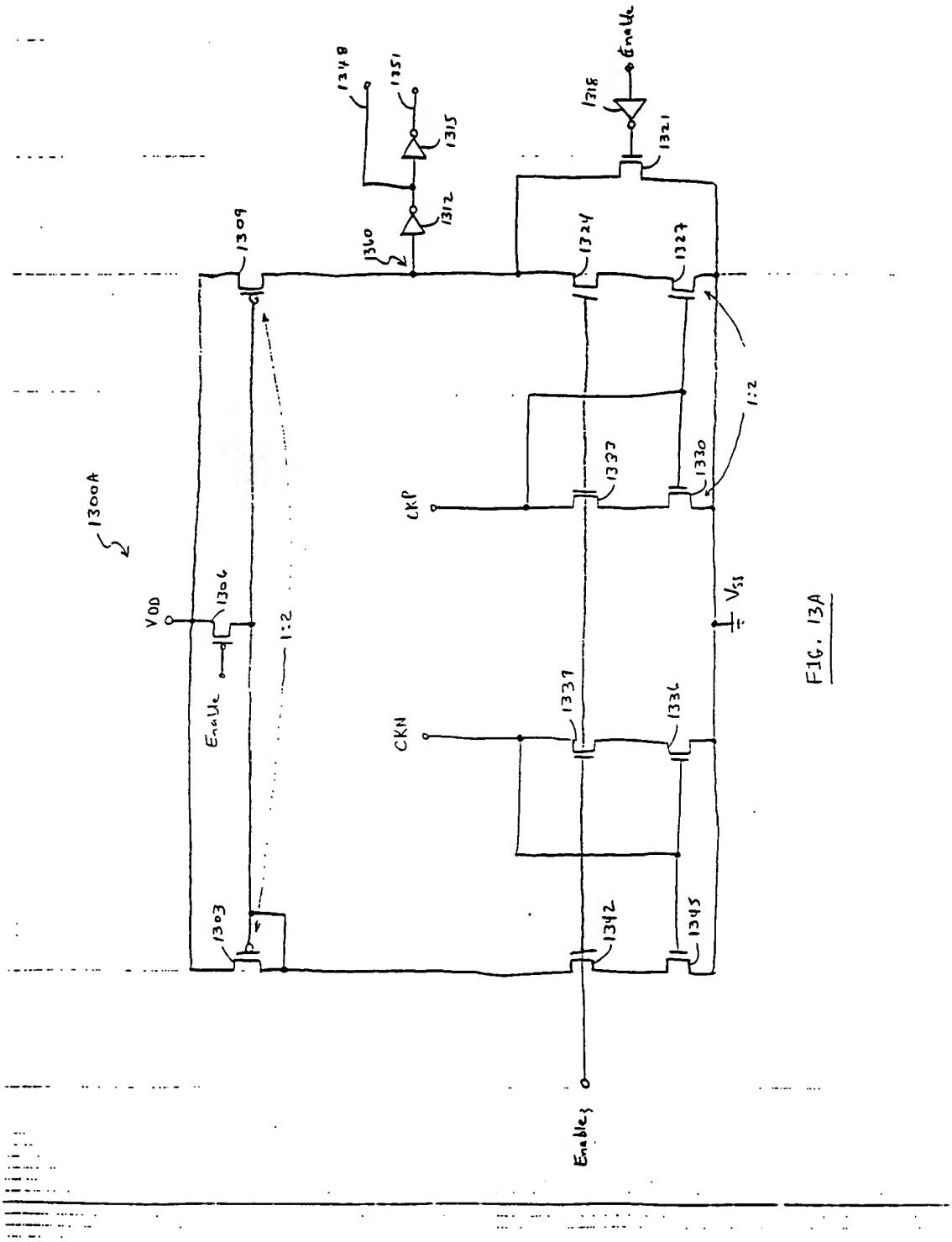
1300A
VDD
1306
Enable
1:2
1303
1309
1340
1348
1351
1315
1312
1318
Enable
1321
1324
1327
1:2
1330
1327
CKP
VSS
1339
1336
CKN
1342
1345
Enables

FIG. 13A

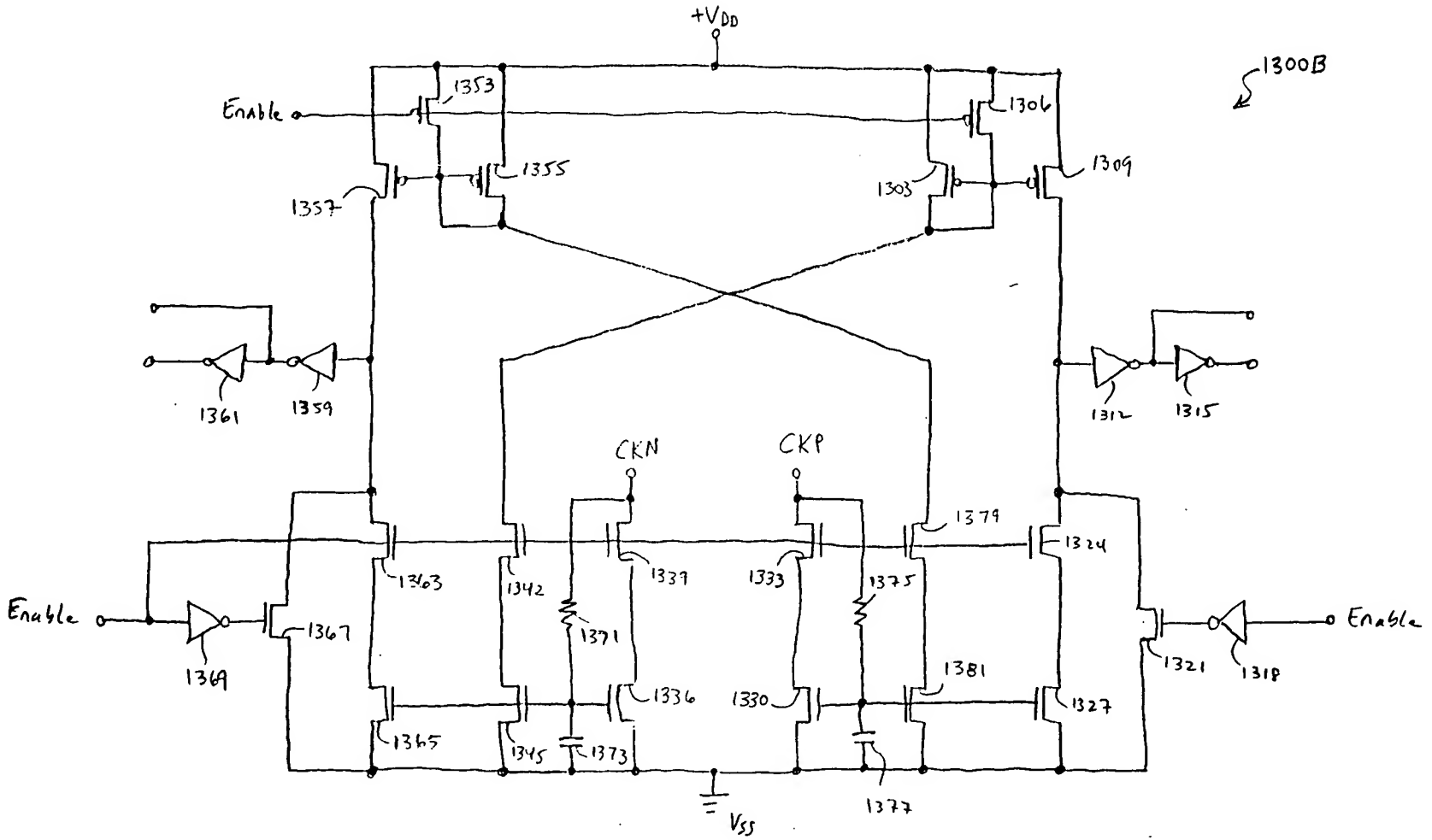
+VDD
1300B
Enable
1353
1306
1355
1309
1357
1303
1361
1359
1312
1315
CKN
CKP
1379
1324
1363
1342
1339
1333
1375
Enable
1367
1371
Enable
1369
1321
1318
1381
1336
1330
1327
1365
1345
1373
1377
Vss

FIG. 13B

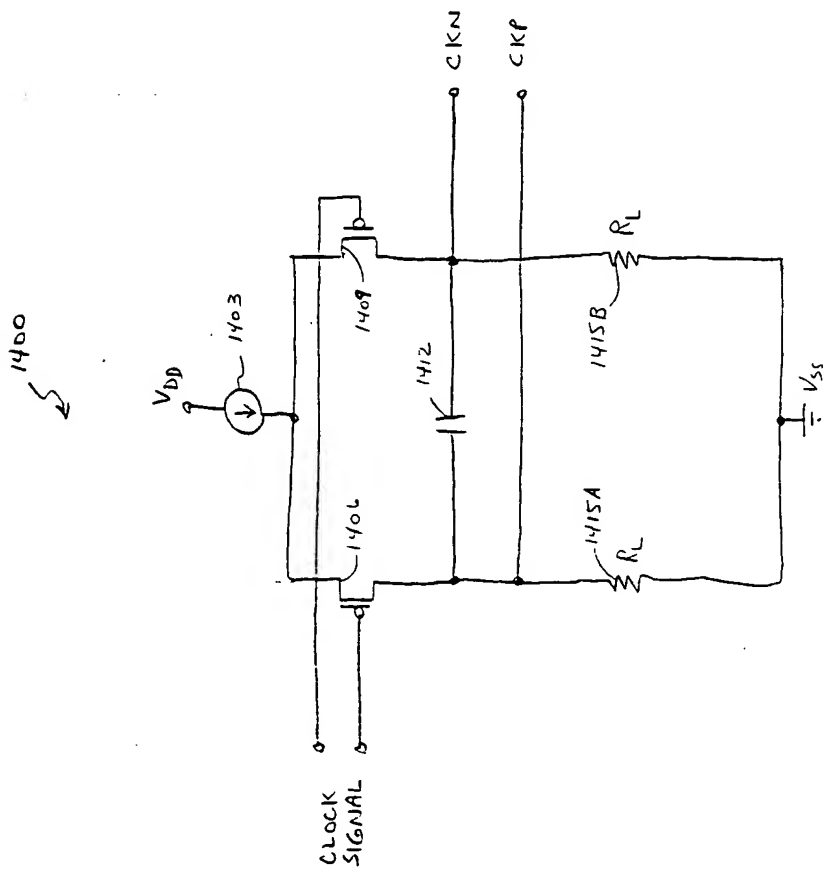
1400
1403
V_{DD}
1409
1412
1406
CKN
CKP
R_L
1415B
1415A
R_L
V_{SS}
CLOCK SIGNAL

FIG. 14

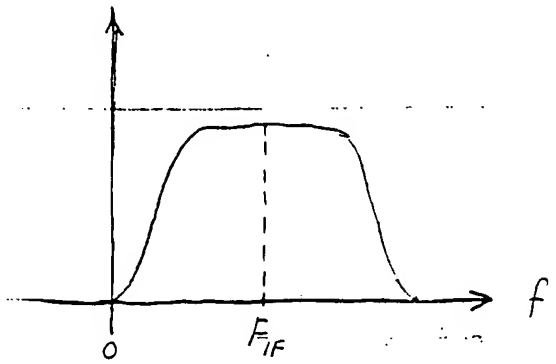
f
0
F_{IF}

FIG. 15

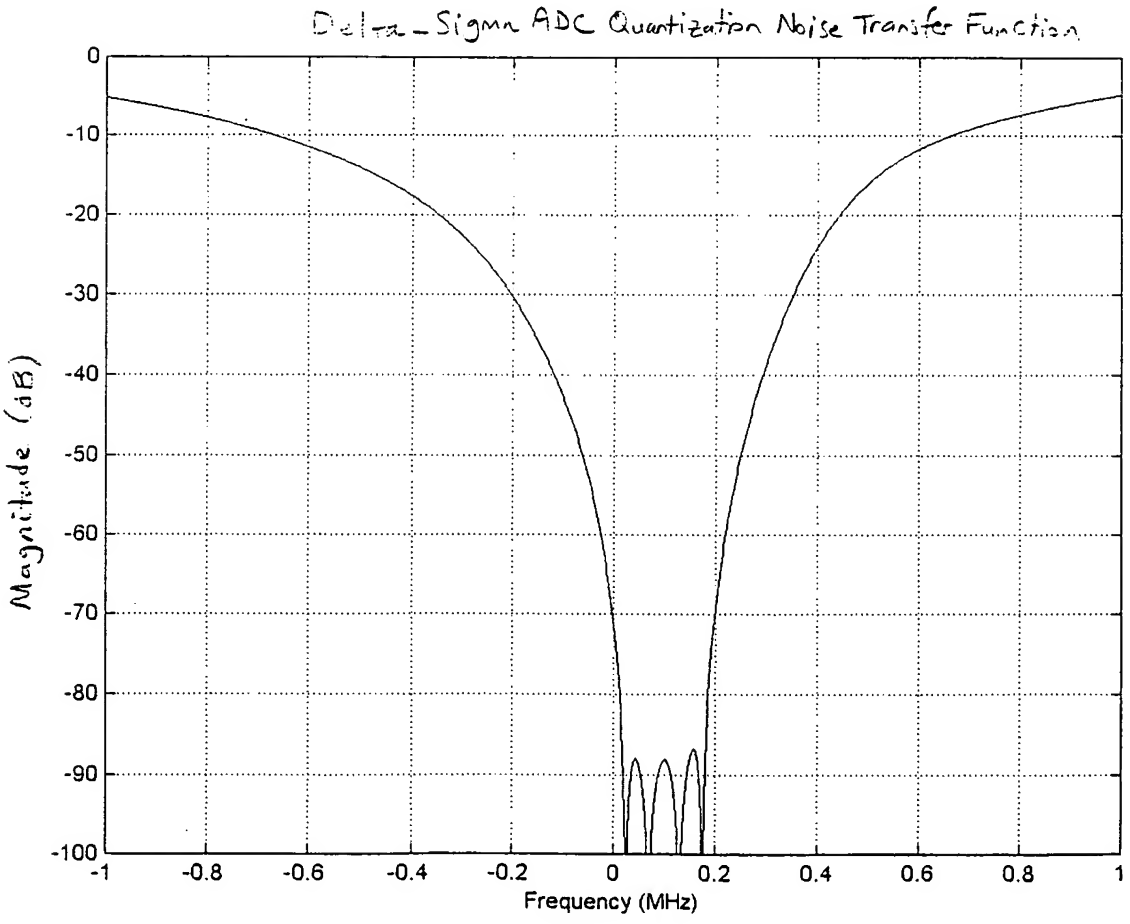
Delta-Sigma ADC Quantization Noise Transfer Function
Magnitude (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
Frequency (MHz)

FIG. 16

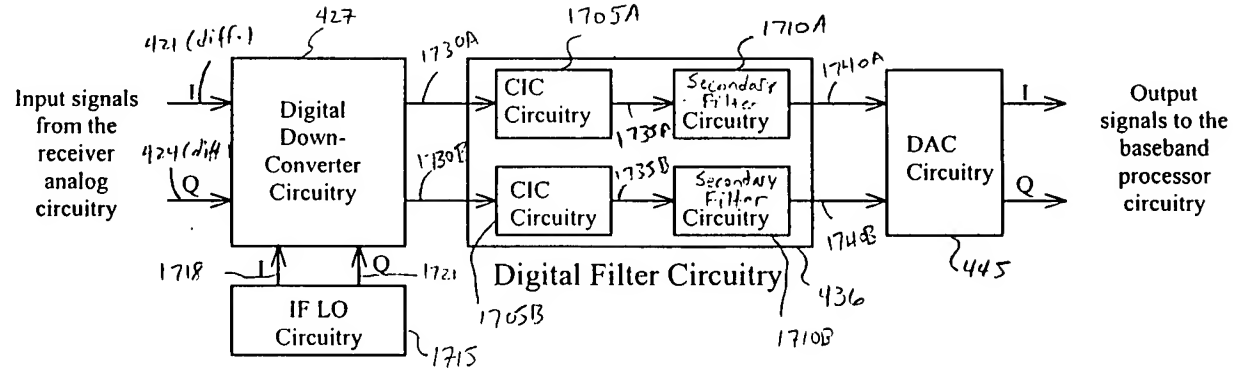

FIG. 17A

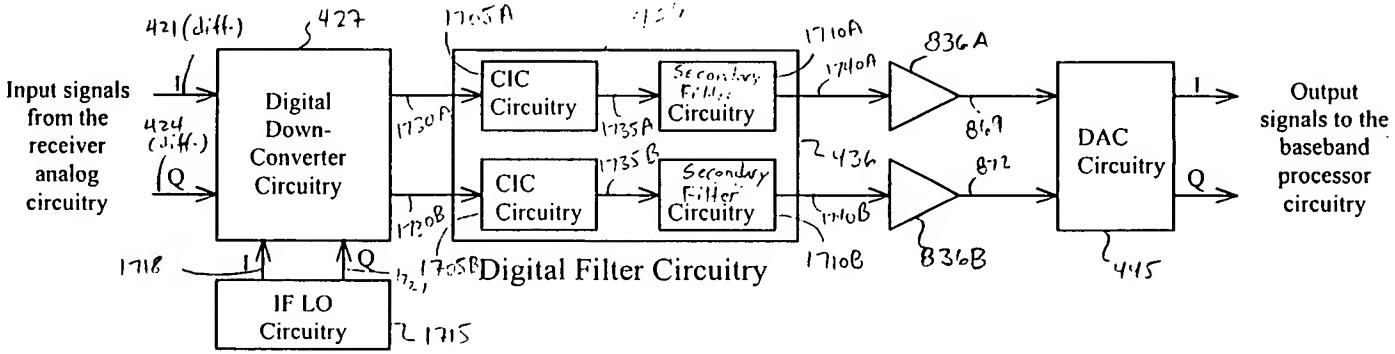

FIG. 17B

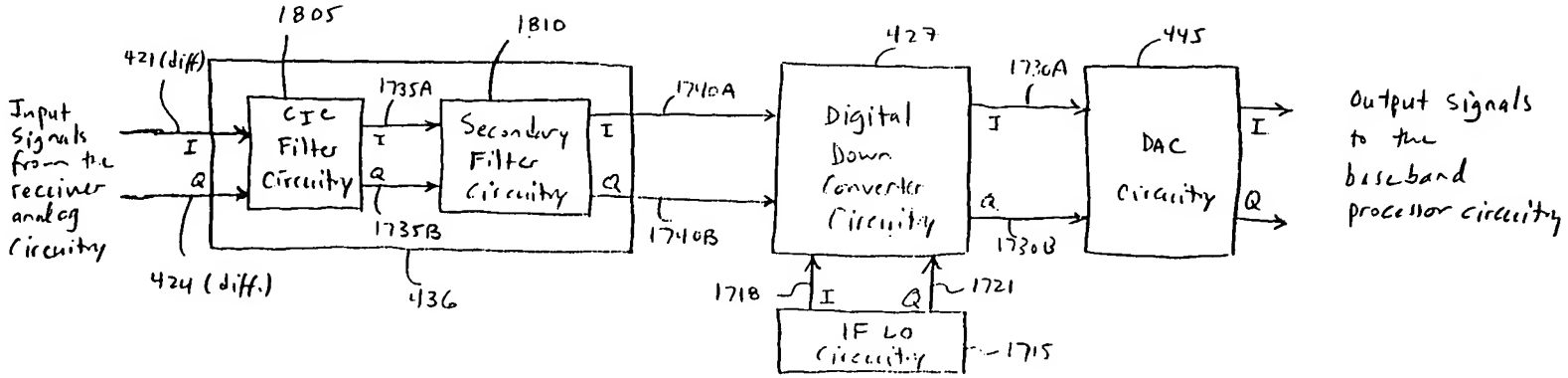

FIG. 18A

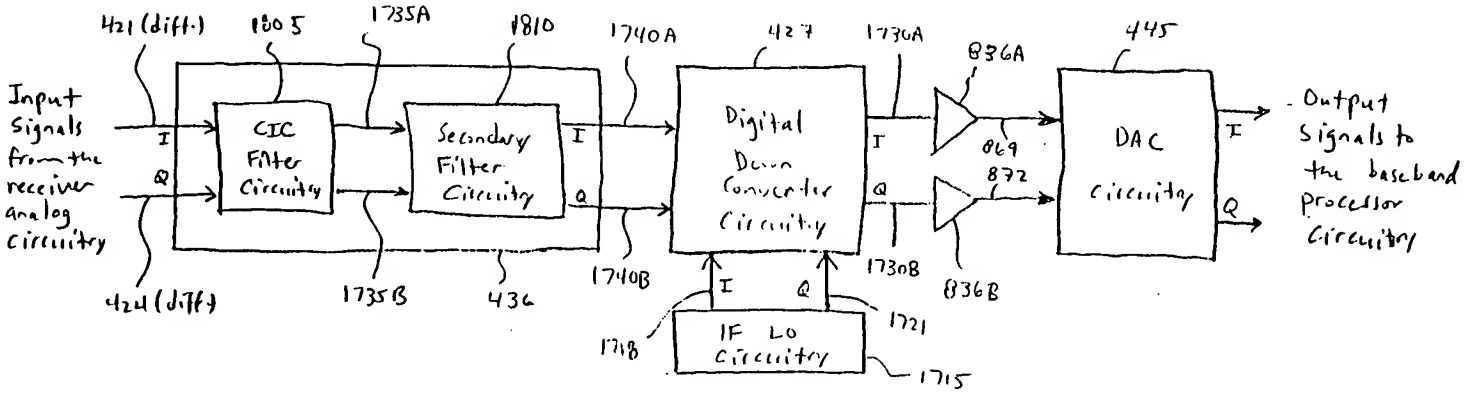

FIG. 18B

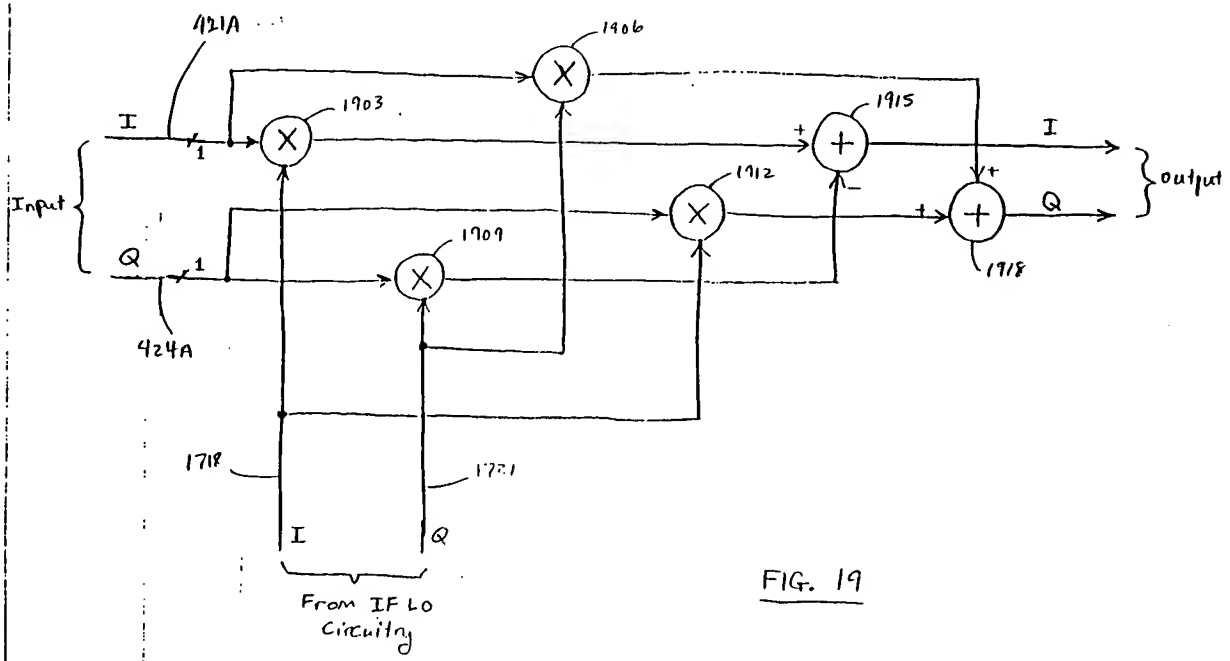
421A
1906
1903
1915
I
Input
1
1912
output
Q
1909
1
Q
1918
424A
1718
1721
I
Q
From IF LO
Circuitry

FIG. 19

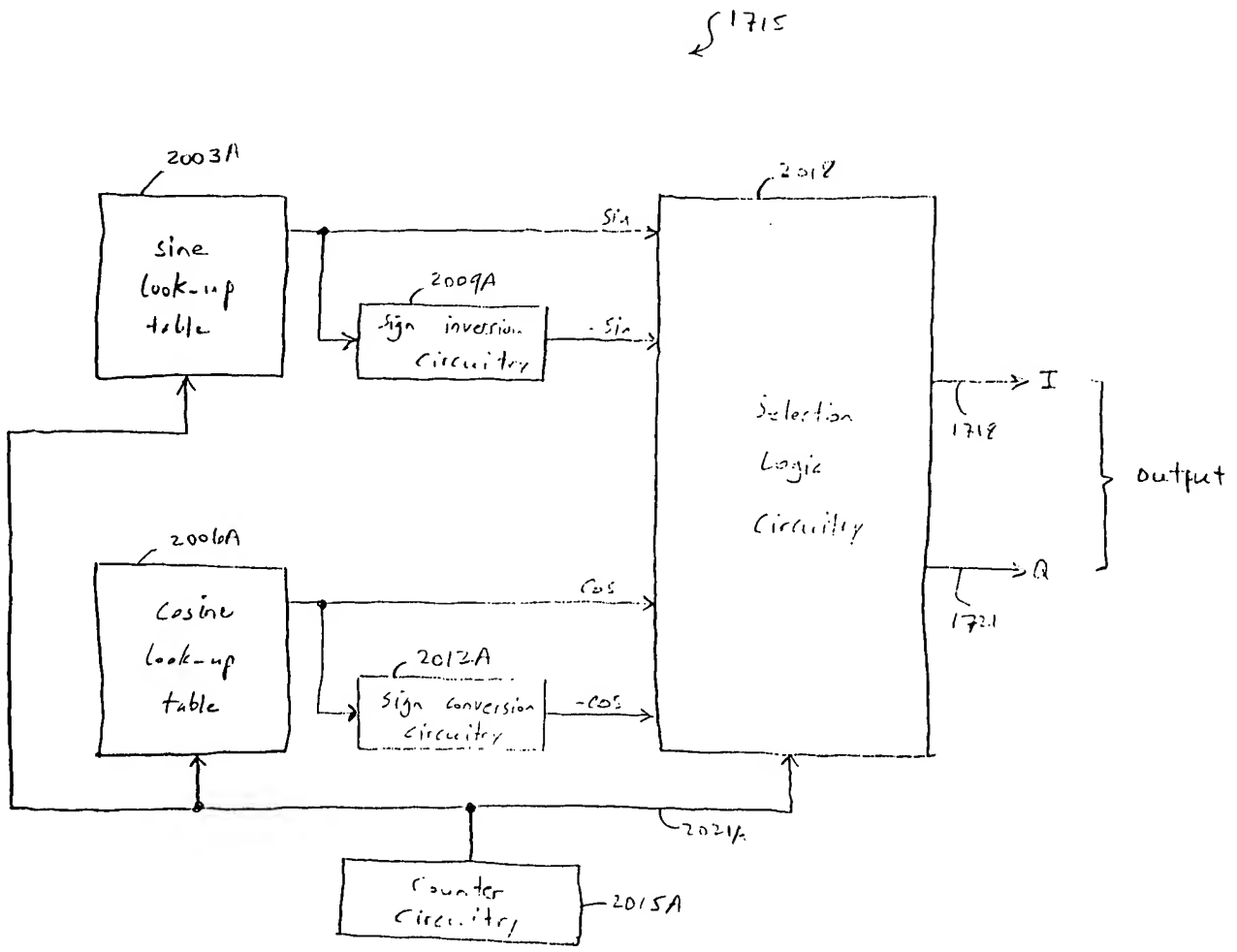
1715
2003A
Sine look-up table
Sin
2009A
Sign inversion Circuitry
-Sin
2018
Selection Logic Circuitry
I
1718
Q
1721
output
2006A
Cosine look-up table
Cos
2012A
Sign conversion circuitry
-Cos
2021A
Counter Circuitry
2015A

FIG. 20A

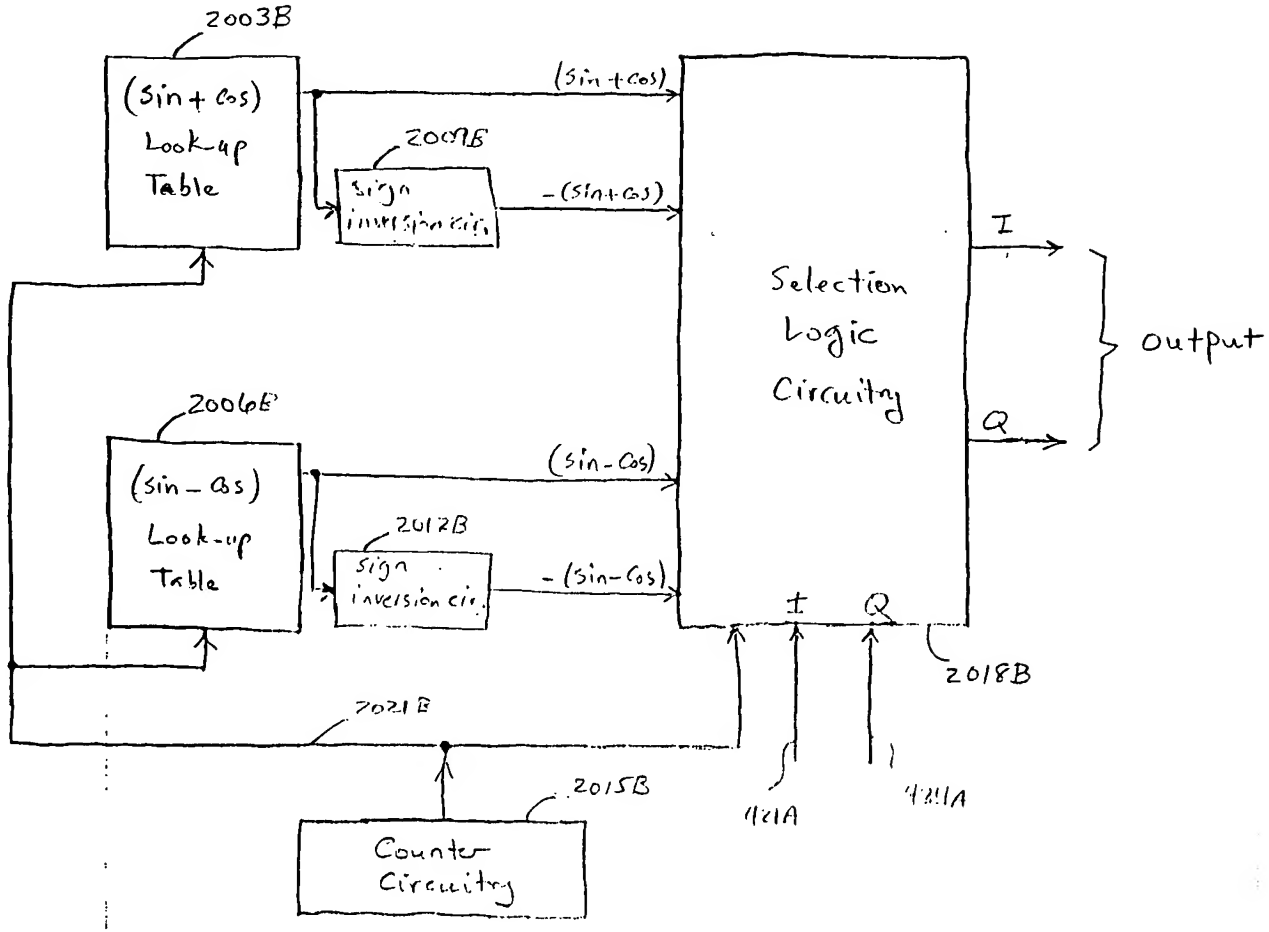
2003B
(Sin + Cos)
Look-up
Table
(Sin + Cos)
2009B
Sign
inversion cir.
-(Sin+Cos)
2006B
(Sin - Cos)
Look-up
Table
(Sin - Cos)
2012B
Sign
inversion cir.
-(Sin-Cos)
Selection
Logic
Circuitry
I
Q
output
±
Q
2018B
2021B
2015B
Counter
Circuitry
421A
421A

FIG. 20B

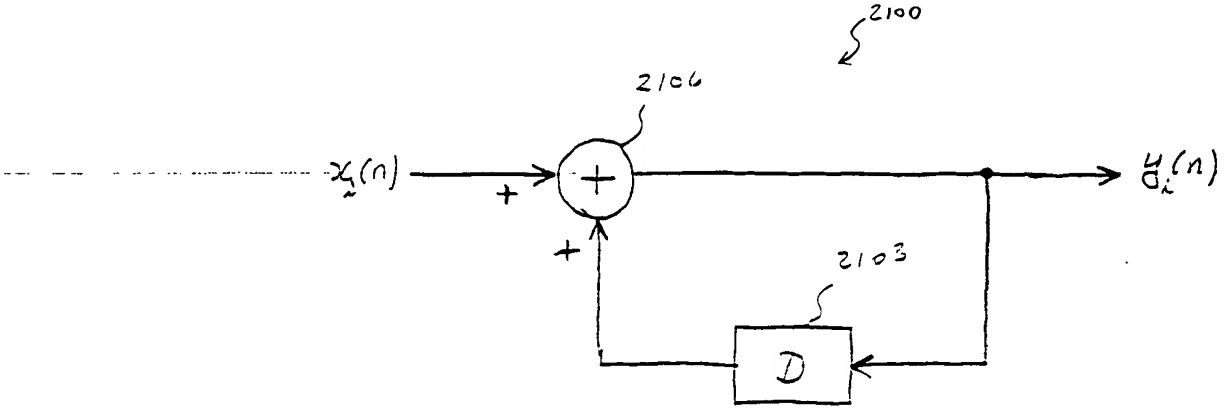

FIG. 21

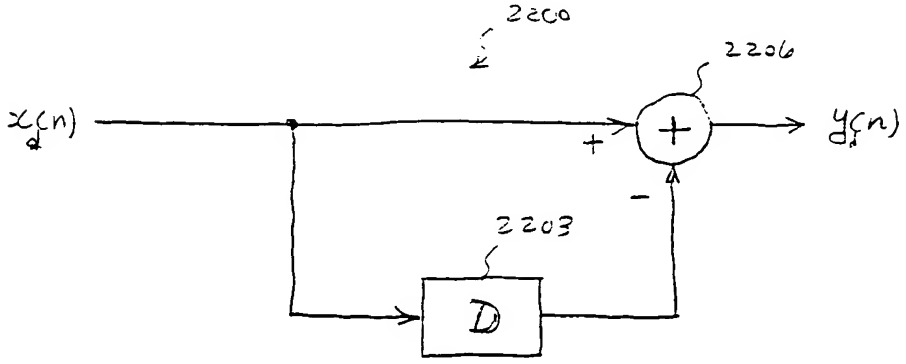

FIG. 22

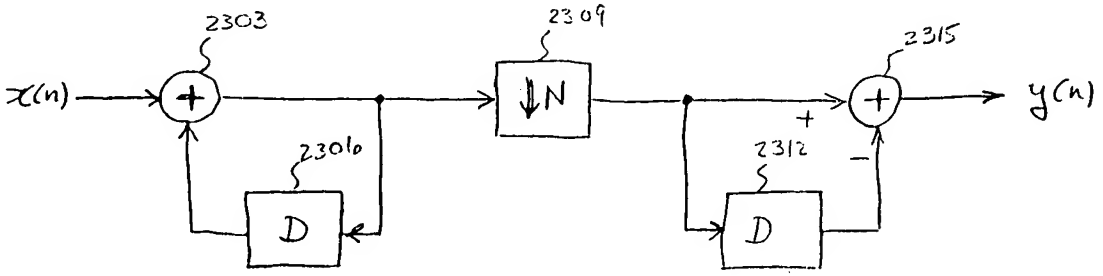
2303
2309
2315
x(n)
N
y(n)
+
2306
2312
−
D
D

FIG. 23

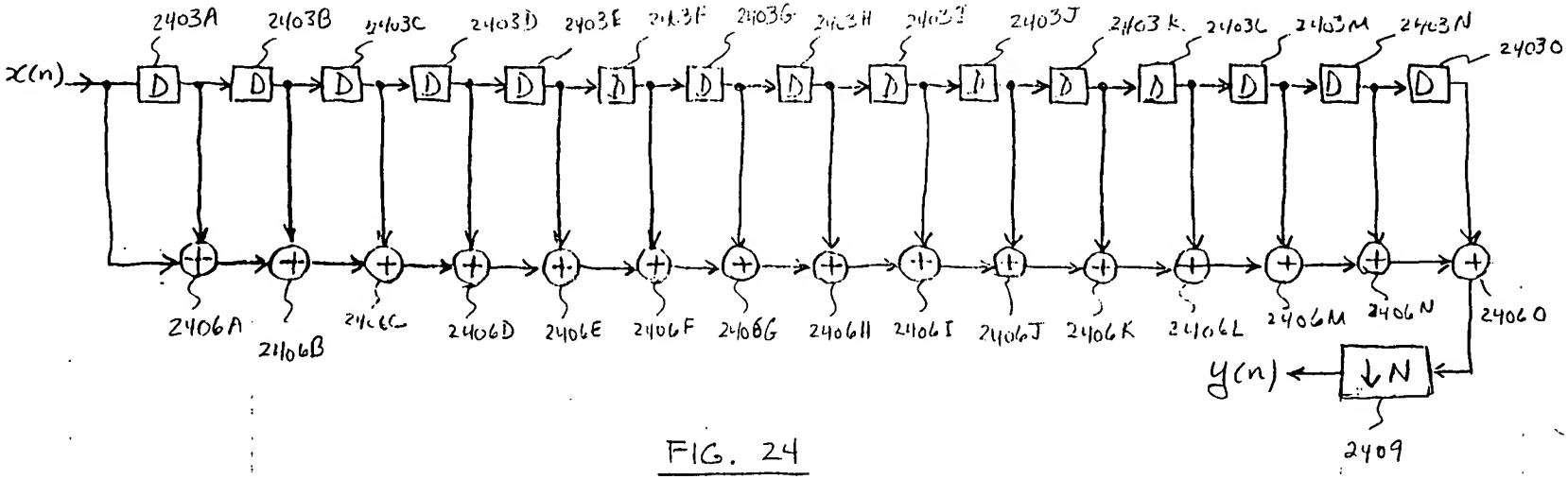
2403A
2403B
2403C
2403D
2403E
2403F
2403G
2403H
2403I
2403J
2403K
2403L
2403M
2403N
2403O
x(n)
D
2406A
2406B
2406C
2406D
2406E
2406F
2406G
2406H
2406I
2406J
2406K
2406L
2406M
2406N
2406O
y(n)
N
2409

FIG. 24

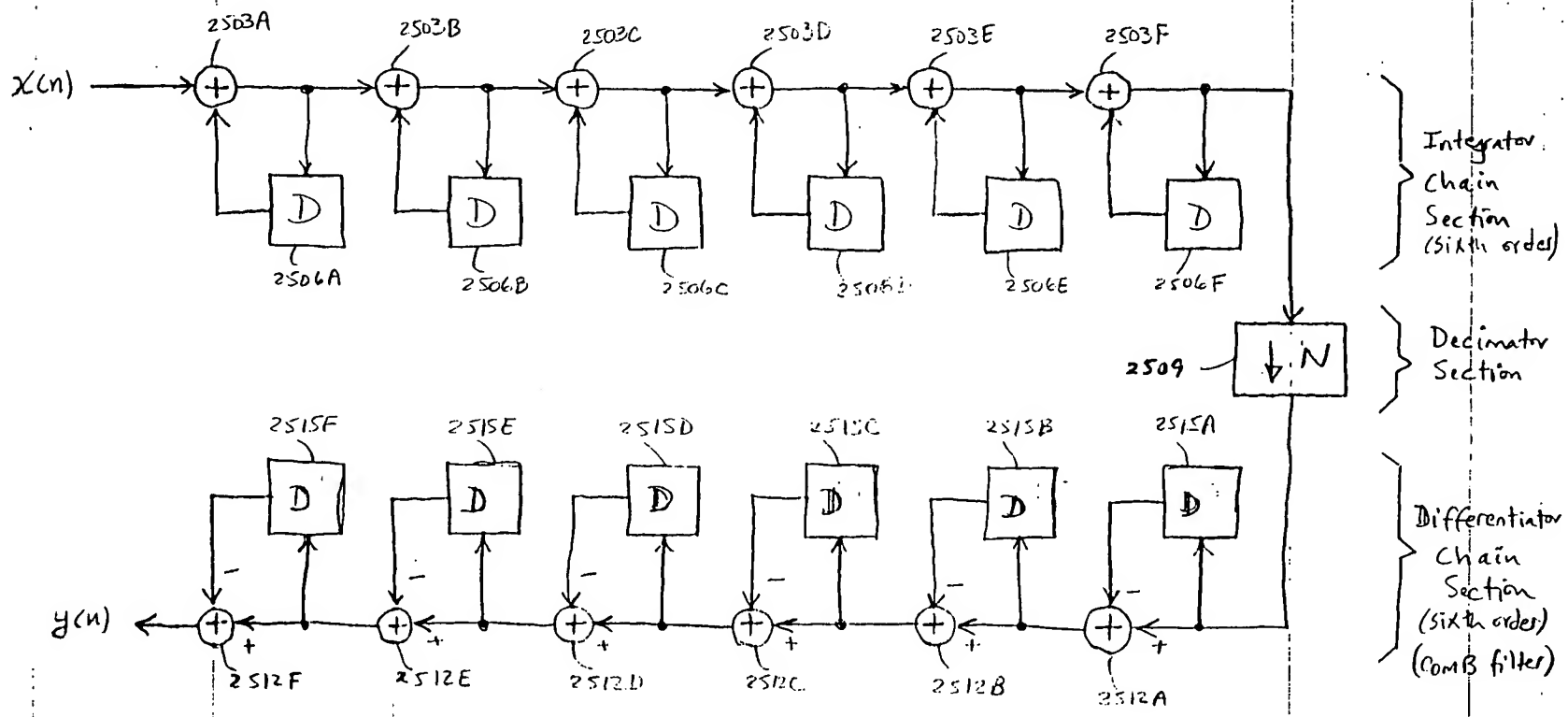
x(n)
2503A
2503B
2503C
2503D
2503E
2503F
D
2506A
2506B
2506C
2506D
2506E
2506F
Integrator Chain Section (Sixth order)
2509
↓N
Decimator Section
2515F
2515E
2515D
2515C
2515B
2515A
Differentiator Chain Section (Sixth order) (Comb filter)
y(n)
2512F
2512E
2512D
2512C
2512B
2512A

FIG. 25

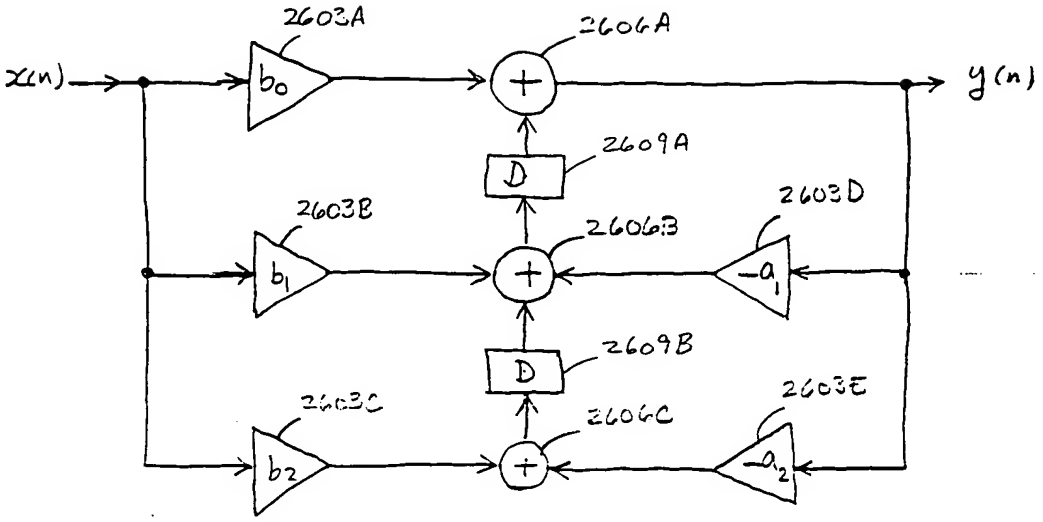
x(n)
2603A
b_0
2606A
y(n)
D
2609A
2603B
b_1
2606B
2603D
$-a_1$
D
2609B
2603C
b_2
2606C
2603E
$-a_2$

FIG. 26

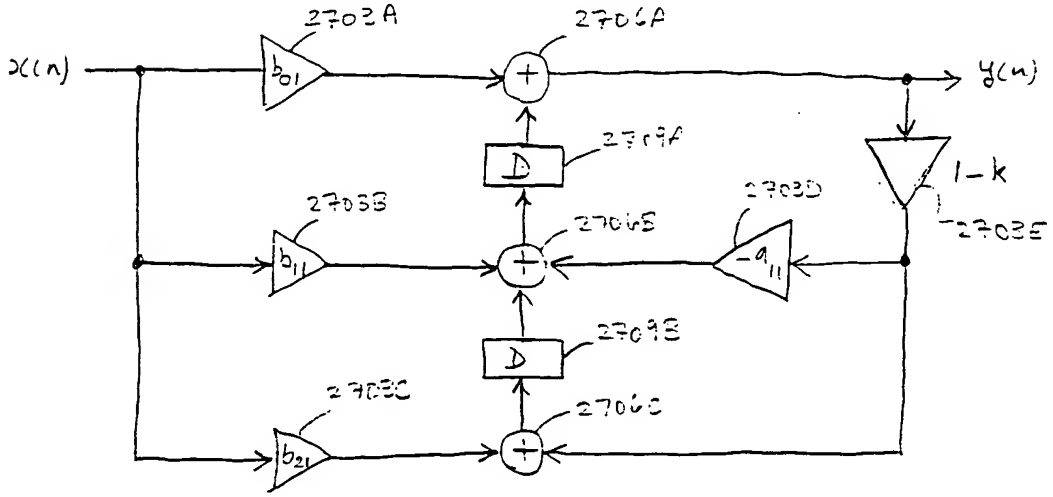
x(n)
2703A
b_{01}
2706A
y(n)
D
2709A
1-k
2703E
2703B
b_{11}
2706B
2703D
$-a_{11}$
D
2709B
2703C
b_{21}
2706C

FIG. 27

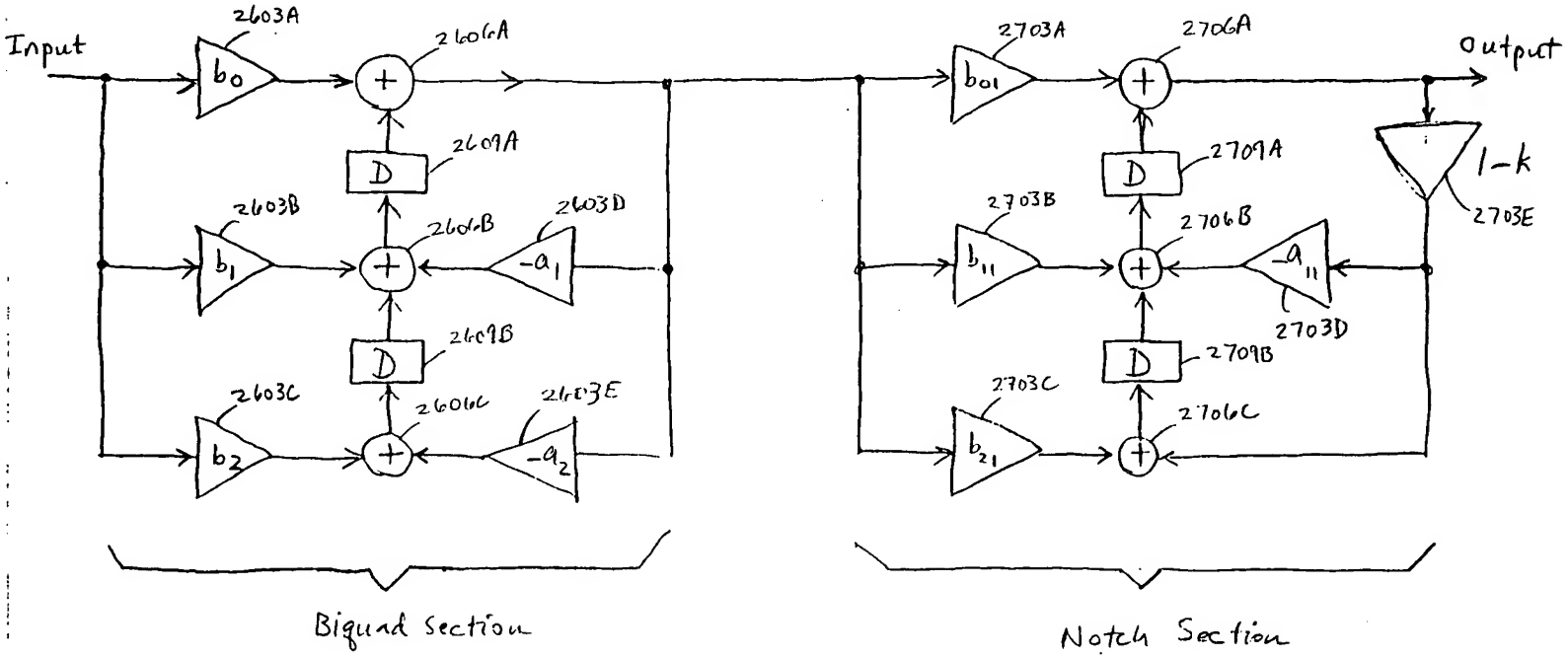
Input
2603A
b_0
2606A
2609A
D
2603B
b_1
2606B
2603D
$-a_1$
2609B
D
2603C
b_2
2606C
2603E
$-a_2$
Biquad Section
2703A
b_{01}
2706A
Output
2709A
D
1-k
2703E
2703B
b_{11}
2706B
$-a_{11}$
2703D
2709B
D
2703C
b_{21}
2706C
Notch Section

FIG. 28A

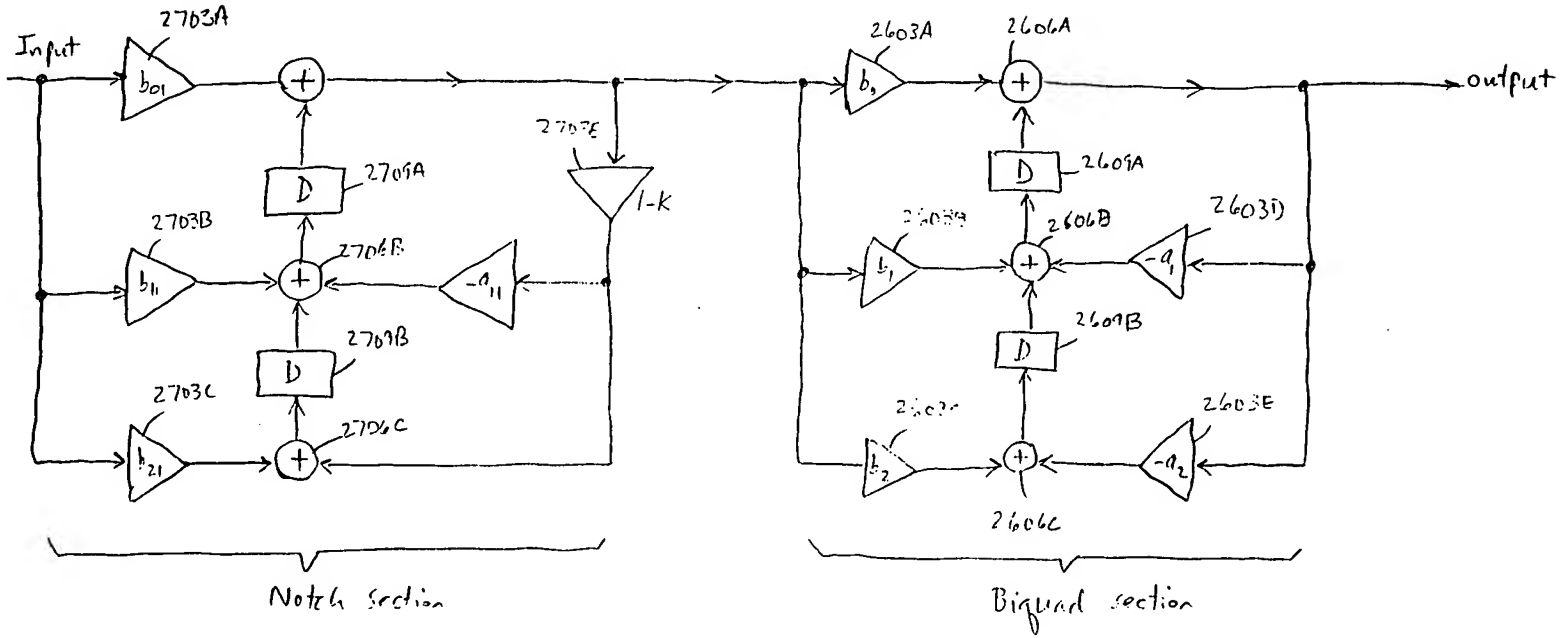
Input
2703A
b_{01}
2709A
D
2703B
b_{11}
2706B
$-a_{11}$
2709B
D
2703C
b_{21}
2706C
2707E
1-K
Notch section
2603A
b_0
2606A
outputt
2609A
D
2603D
2606B
b_1
$-a_1$
2609B
D
2603E
b_2
$-a_2$
2606C
Biquad section

FIG. 28B

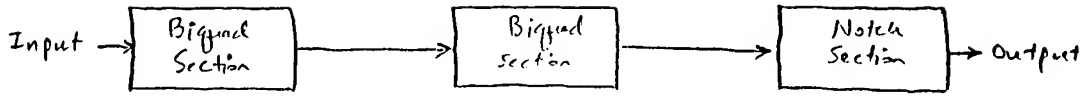

FIG. 29A

FIG. 29B

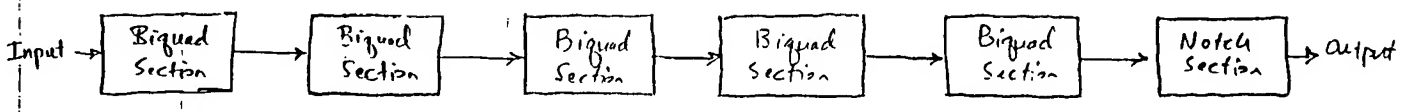

FIG. 29C

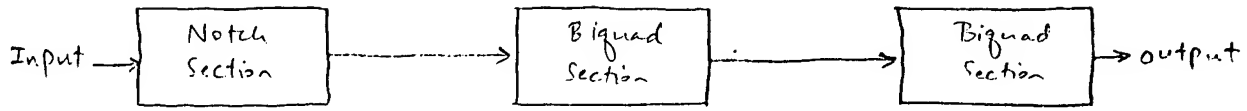

FIG. 29D

FIG. 29E

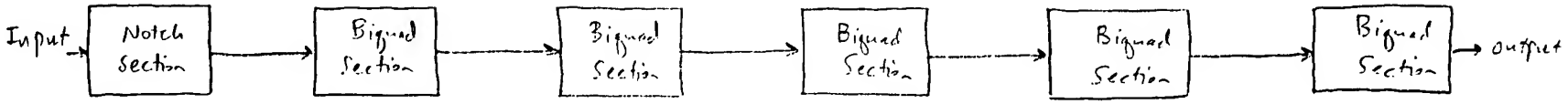

FIG. 29F

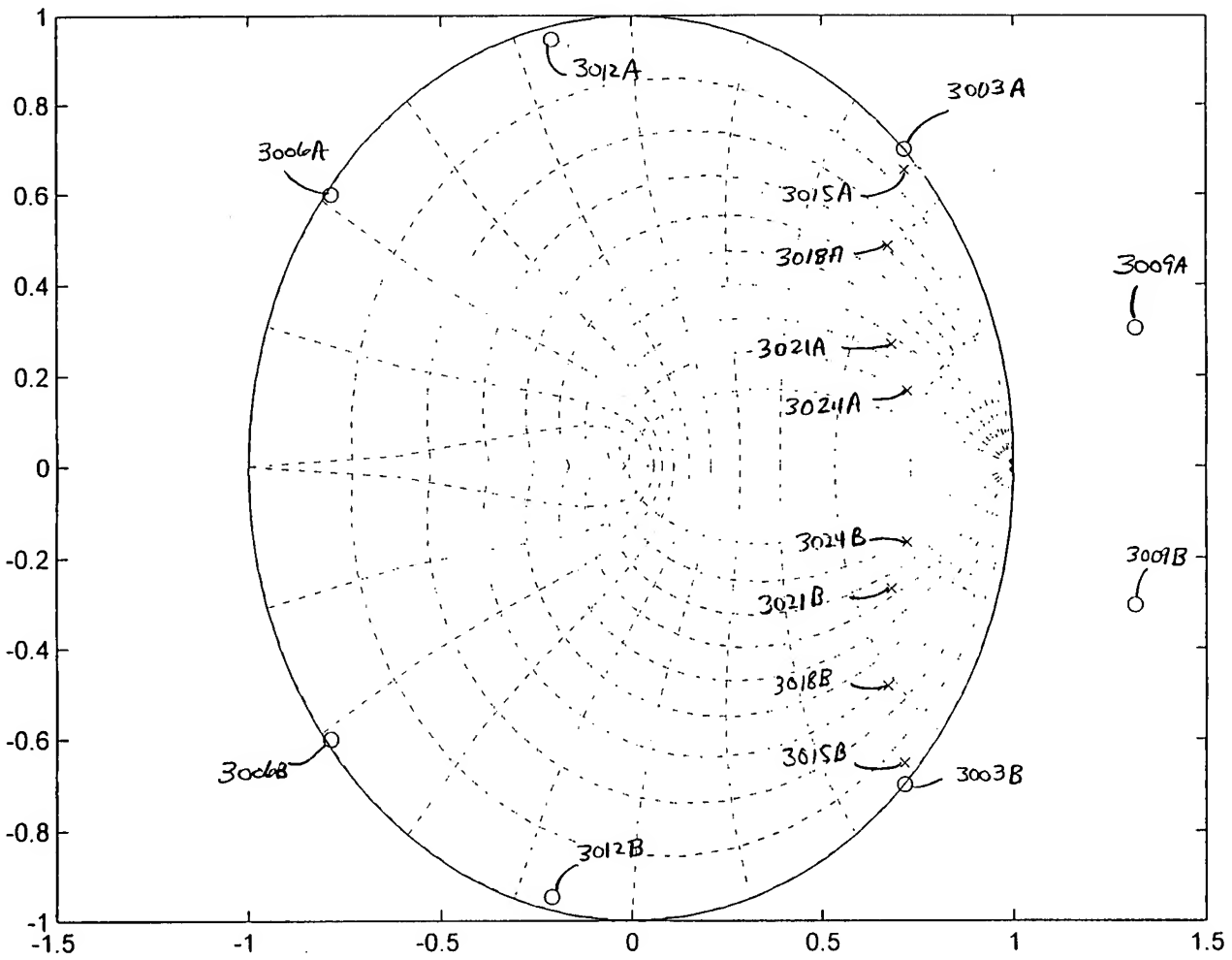
3012A
3003A
3006A
3015A
3018A
3009A
3021A
3024A
3024B
3009B
3021B
3018B
3015B
3003B
3006B
3012B
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-1.5
-1
-0.5
0
0.5
1
1.5

FIG. 30A

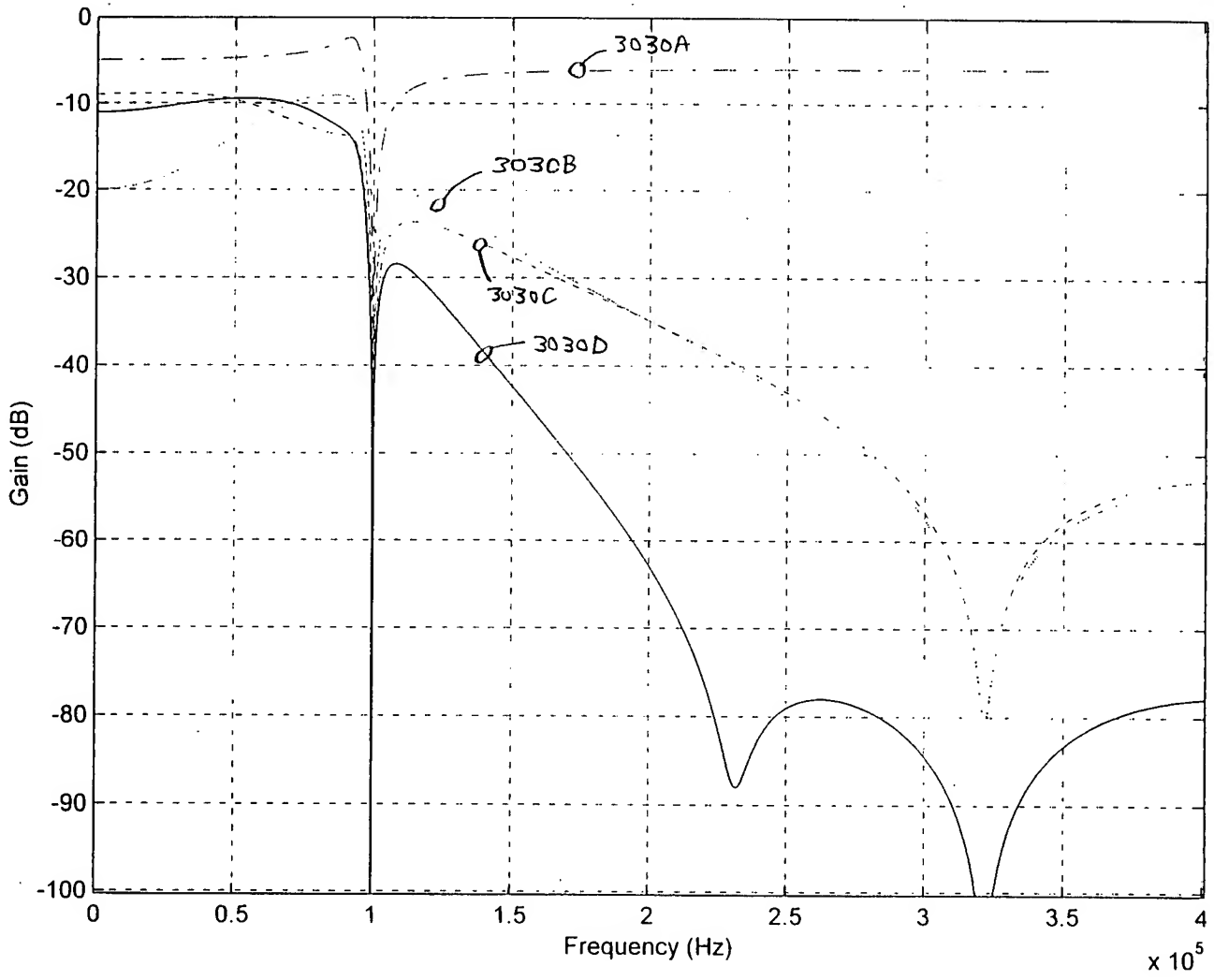
3030A
3030B
3030C
3030D
Gain (dB)
Frequency (Hz)
x 10^5
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
0.5
1
1.5
2
2.5
3
3.5
4

FIG. 30B

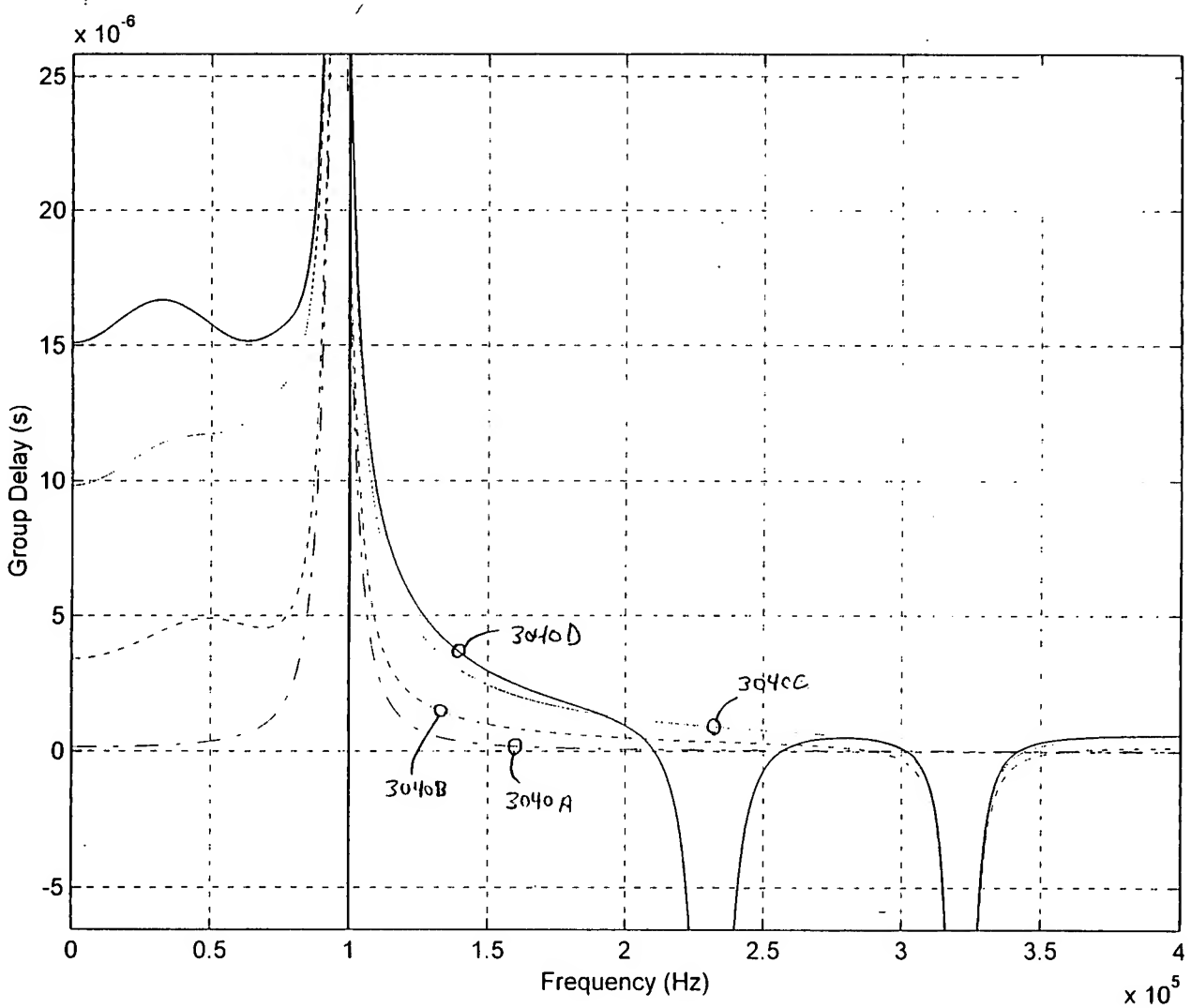
x 10^-6
25
20
15
10
5
0
-5
Group Delay (s)
0
0.5
1
1.5
2
2.5
3
3.5
4
Frequency (Hz)
x 10^5
304D
304C
304B
304A

FIG. 30C

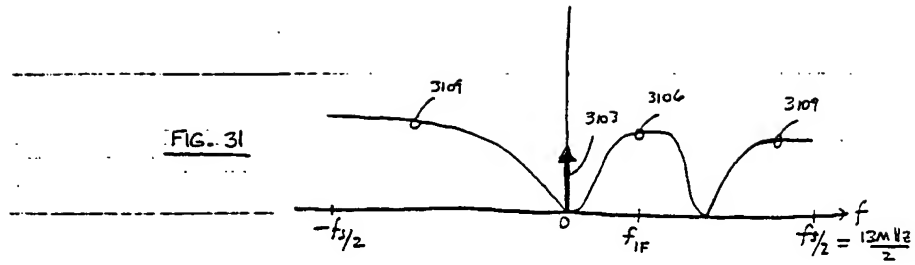

FIG. 31

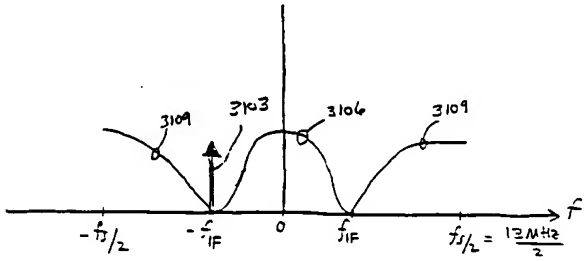

FIG. 32

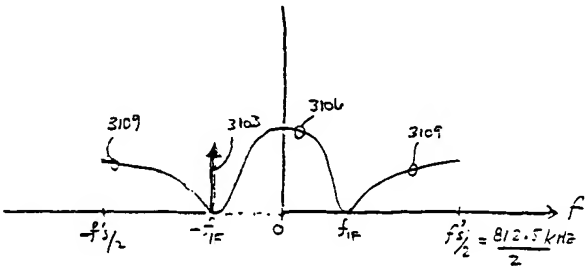

FIG. 33

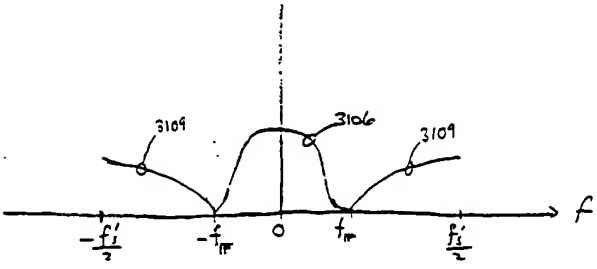

FIG. 34

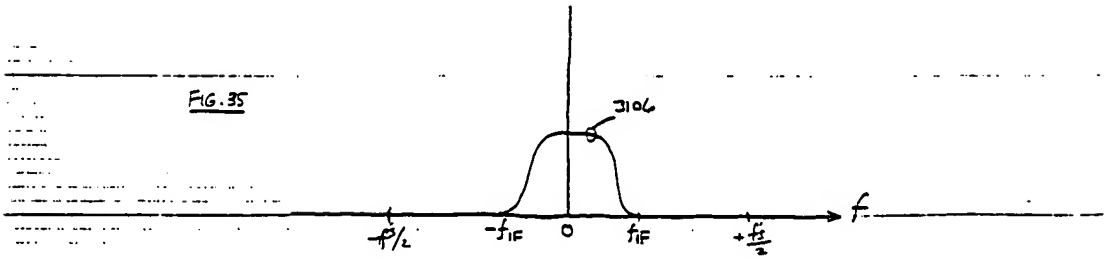

FIG. 35

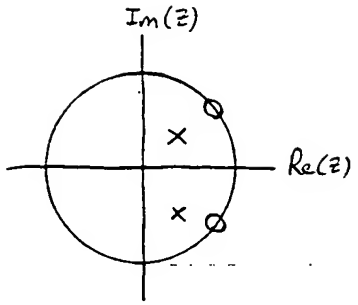

FIG. 36A

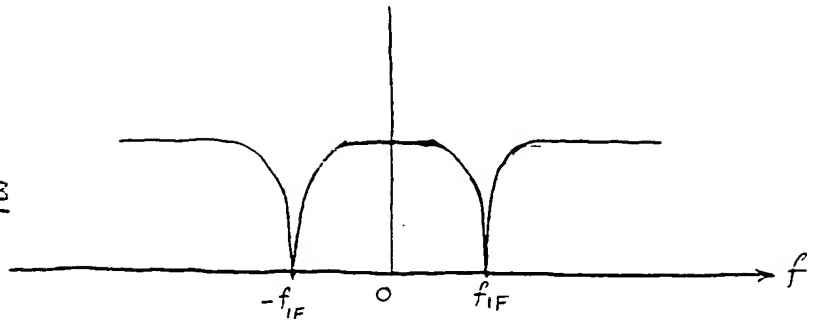

FIG. 36B

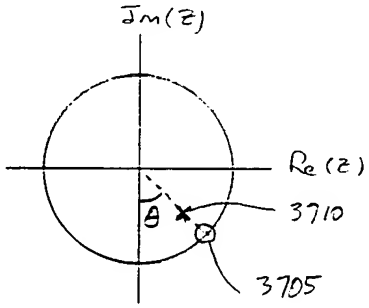

FIG. 37A

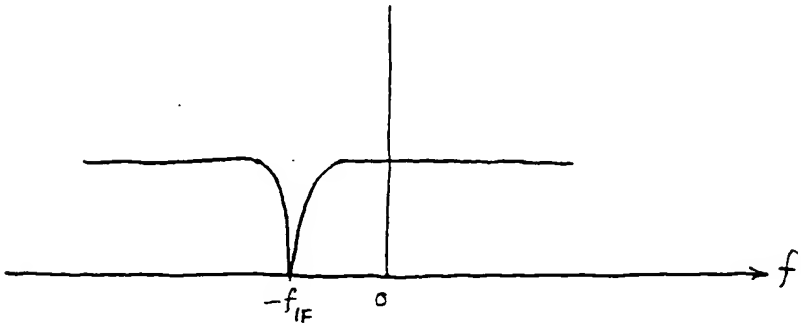

FIG. 37B

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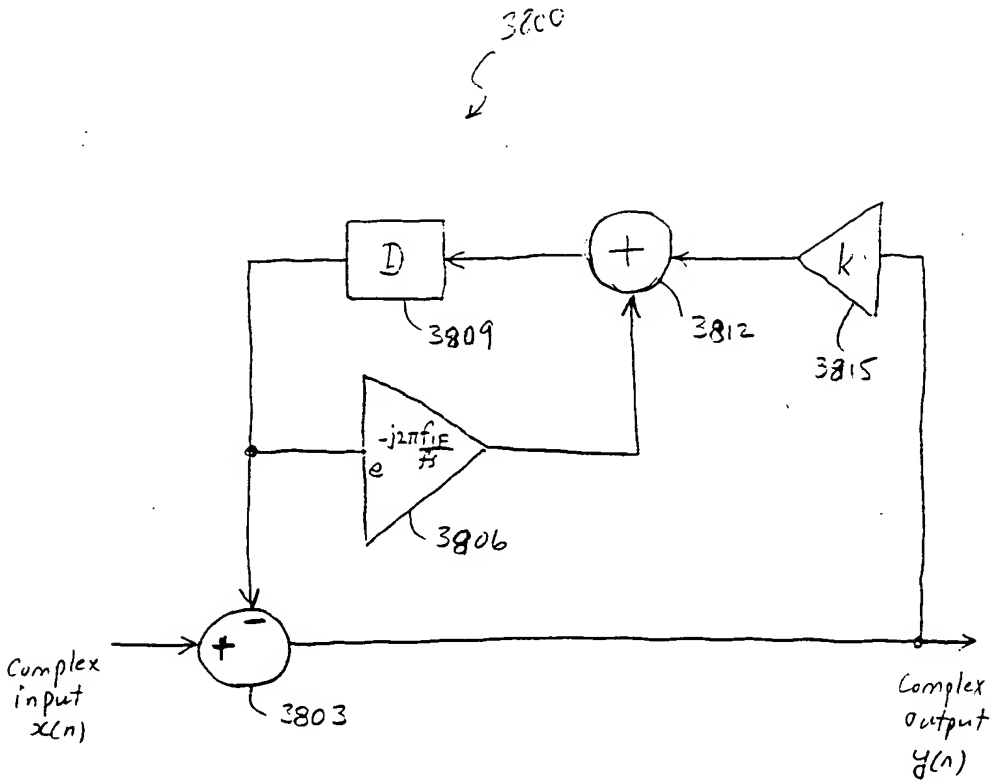

FIG. 38

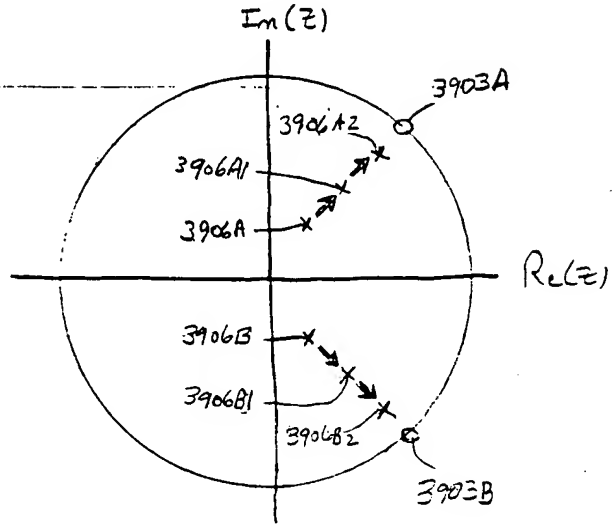
Im(z)
3903A
3906A2
3906A1
3906A
Re(z)
3906B
3906B1
3906B2
3903B

FIG. 39

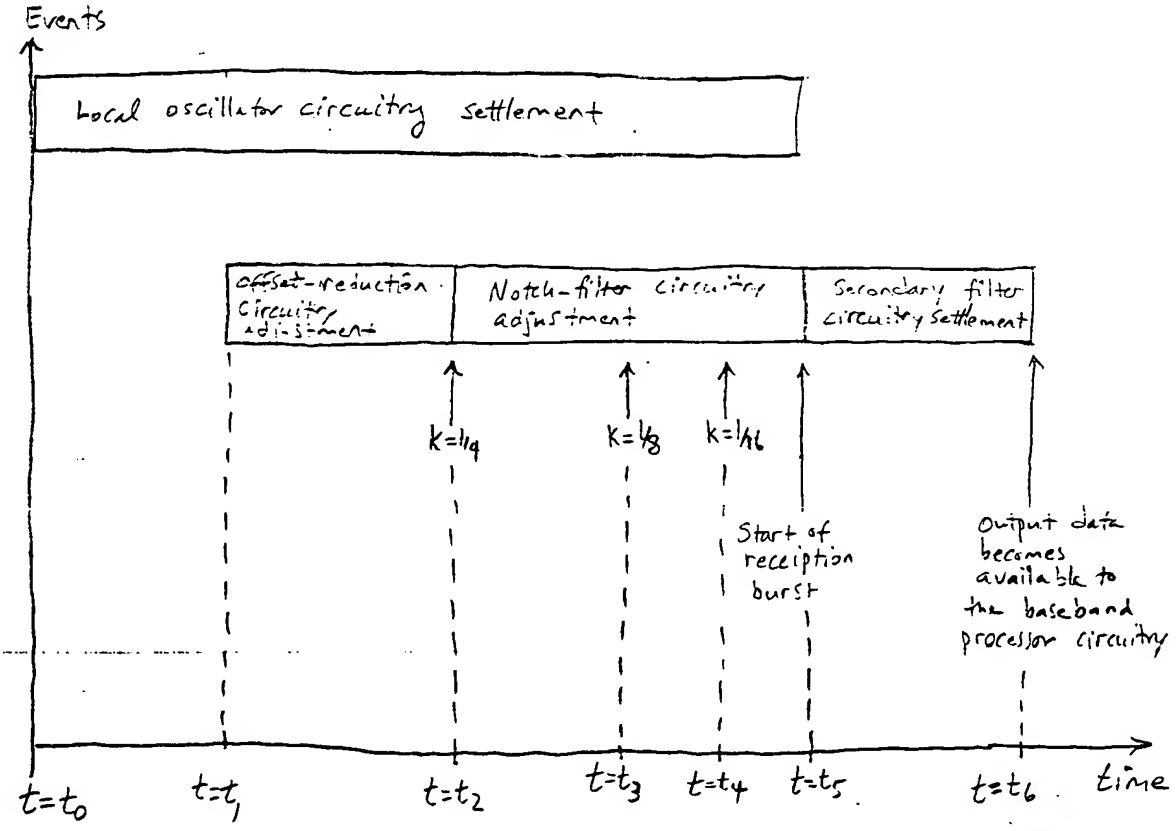
Events
Local oscillator circuitry settlement
offset-reduction circuitry adjustment
Notch-filter circuitry adjustment
Secondary filter circuitry settlement
k=1/4
k=1/8
k=1/16
Start of reception burst
Output data becomes available to the baseband processor circuitry
t=t0
t=t1
t=t2
t=t3
t=t4
t=t5
t=t6
time

FIG. 40